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Analysis of Mechanisms for Hot-Carrier-Induced VLSI Circuit Degradation

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In this paper we detail the mechanism for hot-carrier induced circuit degradation in actual 64Mb DRAM, by investigating the DRAM specification parameter shift due to transistor aging in each of the constituent circuit. It was found that hot-carrier induced transistor aging of the circuit block does not directly affect the internal clock speed degradation, however, it does seriously reduce the design margin of the circuit which suffers from heavy loads.

I. Introduction

During the last decade, hot-carrier degradation has evolved from an academic topic of research to a issue of vital interest for the development of future VLSI technologies. It is recognized today that hot-carrier induced long-term reliability of CMOS VLSI circuits is becoming an important issue as the density of VLSI chips increases with shrinking design rules. Furthermore, in view of a number practical reasons, the most logical scaling theory of device dimension called constant field scaling has been abandoned because of compatibility with TTL-supply voltage, slow-down of circuits due to the non-scaling of parastic capacitances, and non-scaling of threshold voltage and subthreshold slop. In order to estimate integrated circuit reliability, a significant portion of research efforts has focused on innovative wafer-level test structures including; ring oscillators [1]-[3], differential amplifiers [4],[5], and the development of integrated-circuit reliability simulation tools [6]-[8]. However, the true impact of hot-carriers on circuit performance has not been yet studied in detail until now. Recent advances in DRAM technology have made it possible to implement many combinations of analog and digital circuit building blocks on a single chip. In these integrated circuits, a unit circuit building block degraded by hot-carrier stress can be incorporated with the unstressed circuit building blocks, and it may lead to an unforeseen, enhanced circuit performance degradation. For these reasons, it is important to know how overall circuit performance is affected by transistor aging and which transistors are most likely to cause critical circuit performance failures. In this paper, hot-carrier induced performance degradation of various constituent circuits and it's impact on the performance of a 64M DRAM were investigated. In light of our findings a new mechanism for the hot-carrier-induced performance degradation of DRAM circuits is proposed.

II. Experimental Method

The 64Mb DRAM chip used in this study were fabricated using a 0.45μm double metal, CMOS process with conventional oxide-spacer LDD structures. The spacer length is 0.15μm with a peak n- concentration of 5E18/cm^3. The MOSFET dimensions are Tox = 10nm, 2ΔL = 0.15μm, and the minimum channel length of NMOSFET and PMOSFET is 0.5μm and 0.6μm respectively. The overall performance degradation was measured using a Teradyne J937 memory tester after stressing the circuits under active cycling at 6 volts which is 1 volt higher than the burn-in voltage. The test was performed at room temperature. Internal probing of the device's critical path before and after stress was performed using an electron-beam prober, hence we were able to investigate the impact of hot-carriers on each of the circuit elements within the 64M DRAM in addition to the effect on the chip as seen by the end user.

III. Results and Discussion

After stressing an actual 64M DRAM chip under active cycling at Vcc=6V, the active and stand-by current were measured as a function of stress time as shown in Fig. 1.

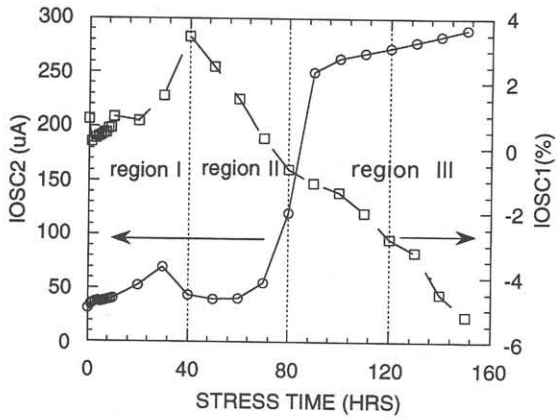


Fig. 1 Active and stand-by current degradation with hot-carrier stress time, of a passivated 64Mb DRAM chip. Iosc1 and Iosc2 means active and stand-by current respectively.

Here, three regions are defined corresponding to different damage regimes. In region I, the active current increases mainly due to the increased driving capability of PMOSFET and the increase of overlap current component caused by degraded slop of inverter output resulting from the different amount of hot-carrier induced degradation in NMOSFET and PMOSFET. As stress time increases further (region II and III), the active current starts to decrease. This phenomena is mainly due to the decrease of driving capability of NMOSFET. However, this result is contradictory to the previous results [9], where the active current decreases until 45 hours, and as stress increases further, the active current starts to increase. This contradictory result can probably be partly ascribed to passivation layer effects in DRAM. While

we used the passivated DRAM in this experiments, there had been no passivation layer in the previous experiment. The TTL stand-by current increases after stress as shown in Fig. 1. The increase of stand-by current after stress in region I and region II is mainly due to the increase of saturation region sub-threshold leakage current in transistors after stress. The increase of saturation region sub-threshold leakage current results in the positive charge injection into the substrate and it can cause substrate potential fluctuation. Hence the steep increase of stand-by current at the end of region II can be attributed to the increase of the total number of charge pumping of the back-bias generator in stand-by mode.

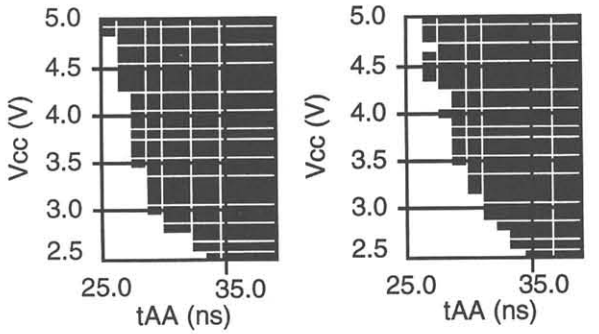


Fig. 2 The t_{AA} schmoo plot of the 64Mb DRAM chip before and after stress.

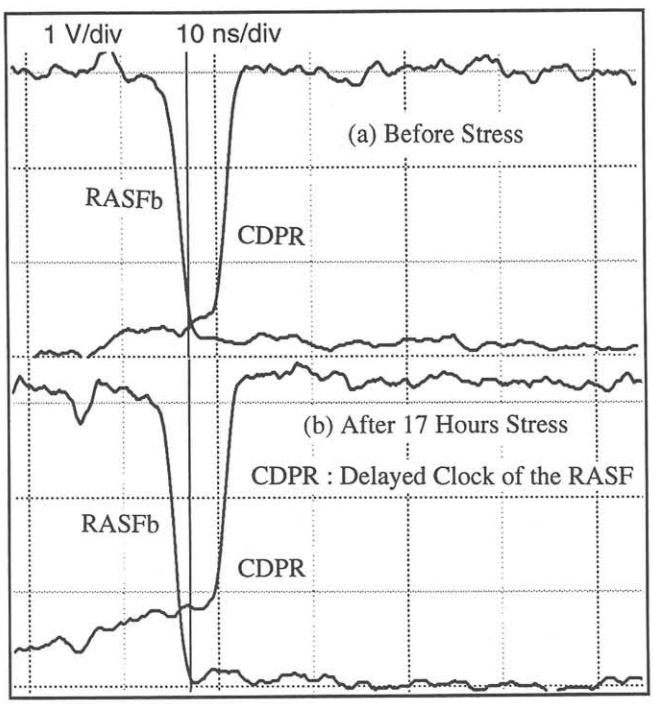


Fig. 3 The internal probing of the /RAS clock before and after 17 hours stress.

The t_{AA} (Access Time from Y-Address) schmoo plot in Fig. 2 shows the speed degradation observed after stress. The cause of this speed degradation, is seen from the internal probing of the critical signal path in 64Mb DRAM.

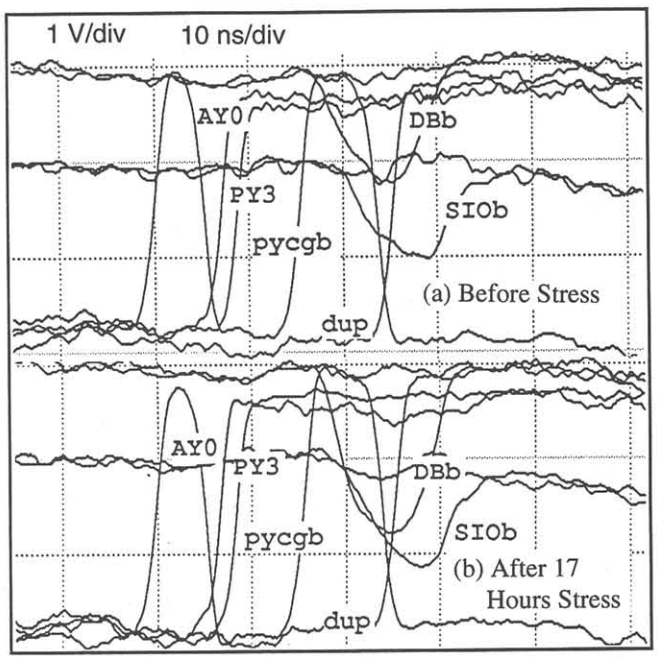


Fig.4 The internal probing results of the data path which determines the column access time (t_{AA}).

Fig. 3 shows one of the /RAS (Row Address Strobe) clock before and after stress. Note that the input-output response delay time of the RASF decreases after stress. Fig. 4 shows the internal probing results of data path which determines the column access time (t_{AA}) indicate that the constituent circuit blocks in t_{AA} path were not affected by hot-carrier stress.

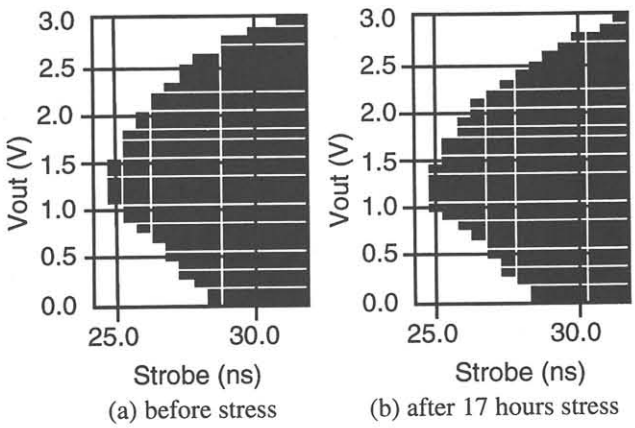
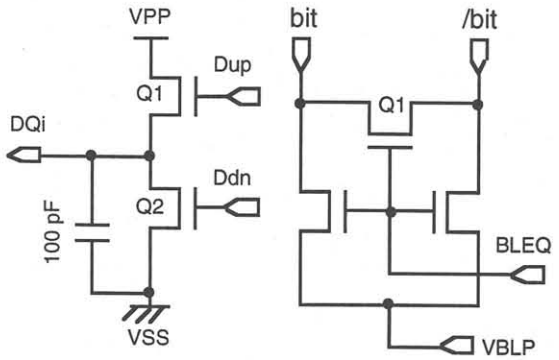


Fig. 5 The output voltage (Vout) schmoo plot before and after 17 hours stress.

The output voltage (Vout) schmoo plot in fig. 5 shows the V_{OH} (Output High Voltage) degradation after stress. It suggests that V_{OH} degradation is responsible for the t_{AA} speed degradation after hot-carrier stressing and that this degradation is caused by aging of the ESD (ElectroStatic Discharge) protection transistor Q1 of the Dout driver in Fig.6(a). The rising time of the Dout signal of the Dout driver circuit is generally designed longer than 4ns in order to reduce the power bouncing. Thus, the pull-up transistor Q1

in Fig. 6(a) suffers from heavy output load. In consequence, the small degradation of the performance of the pull-up device Q1 directly affected the output characteristics of the Dout driver.



(a) Data Output Buffer (b) Bit Line Precharge Circuit

Fig. 6 Data output buffer and bit line precharge circuitry in 64Mb DRAM used in experiment.

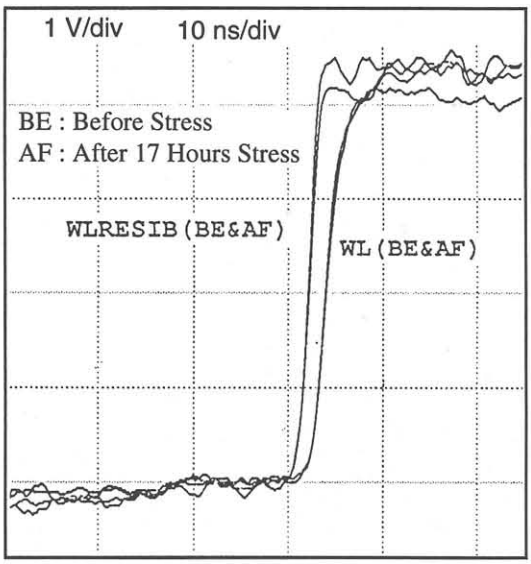


Fig. 7 The internal probing of the waveform of the W/L and WLRESIb operated by V_{PP} (V_{CC}+2Vth).

Fig. 7 shows the waveform of the word line (W/L) and control signal (WLRESIb) operated by V_{PP} (V_{CC}+2Vth). Note that they does not change after stress. Thus, the generally accepted concern that circuits operated by higher voltage are more degraded appears to be too simplistic. Circuit performance degradation caused by hot-carrier stress depends more on the circuit structure used including the output loading of that structure.

Finally, Fig. 8 shows the /RAS precharge time (t_{RP}) schmoo plot before and after stress. This specification parameter determines how fast the bit lines are precharged before the next cycle of operation begins. Consider a typical precharge circuit used in 64Mb DRAM, as shown in Fig.6(b).

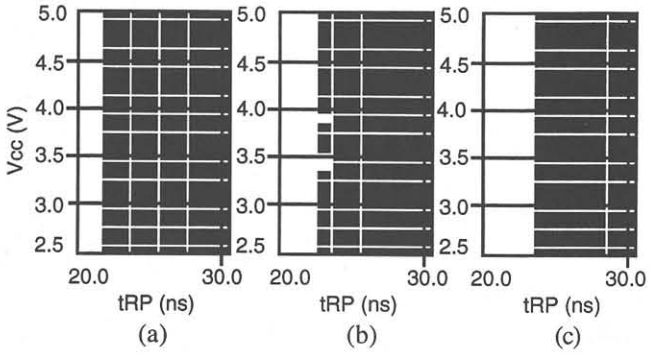


Fig. 8 The t_{RP} (/RAS precharge time) schmoo plot of of the 64Mb DRAM chip. (a) before stress (b) after 17 hours stress (c) after 47 hours stress

If the clock BLEQ goes high in precharge time, the device Q1 which equalizes the bit line and /bit line suffers from hot-carrier stress. Thus, the performance of transistor Q1 is degraded due to hot-carrier stress in precharge period. It would take longer to equalize both the bit lines, consequently the t_{RP} characteristic would be degraded. This degradation in t_{RP} is caused by the degradation in the linear region drive current of the Q1 transistor in Fig. 6(b).

IV. Conclusions

The impact of hot-carriers on VLSI circuits was studied by stressing an actual 64M DRAM chip. Both overall circuit degradation measured on a memory tester, and the internal performance of circuit blocks within the DRAM were thoroughly investigated by electron-beam prober. It was found that hot-carrier-induced device degradation in the circuit does not always directly affect the internal clock delay, but narrow down the design margin of the circuit block with heavy output load. Hot-carrier-induced circuit degradation depends more on the circuit structure rather than on the voltage level. To improve hot-carrier immunity of VLSI circuit, it is very important to find out the least hot-carrier immune unit circuit in the VLSI circuit and to understand the overall circuit degradation mechanism as a function of individual transistor degradation.

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