Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 815-817

Large 1/f Noise in Polysilicon TFT Loads and Its Effects on the Stability of SRAM Cells

Masaaki Aoki, Takashi Hashimoto*, Toshiaki Yamanaka and Takahiro Nagano*
Central Research Laboratory, Hitachi, Ltd.
1-280, Higashi-koigakubo, Kokubunji, Tokyo 185, Japan
*Semiconductor and Integrated Circuits Division, Hitachi, Ltd.

We have observed very large drain current fluctuations over time in polysilicon TFTs. The noise with 1/f power spectra in TFTs is found to be about 10^4 times larger than that of single-crystalline Si MOS transistors. The influence that 1/f noise in TFTs has on SRAM cell stability is clarified for the first time in this paper. On-current improvement and lowering of the grain-boundary barrier are found to be essential to increase stablity.

1. INTRODUCTION

Polysilicon thin-film transistor (TFT) load has recently become a key device technology for high density SRAM cells [1, 2] (Fig. 1) due to their low standby power dissipation and high on/off current ratio. Stacking polysilicon TFT loads over active driver transistors also allows very high integration density. Very large 1/f noise, however, has been observed in polysilicon TFTs [3]. The purpose of this paper is to clarify the effects that noise in TFTs has on cell stability and provide a design principle for stable TFT load cells.

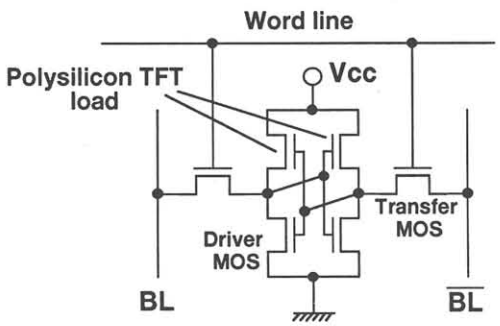

Fig. 1 Equivalent circuit of SRAM cell with polysilicon TFT loads.

2. EXPERIMENTAL

The polysilicon TFT samples for measurements of drain current and gate voltage fluctuations have both top-gate and bottom-gate structures, as shown in Fig. 2. Active polysilicon films below 50 nm thick were deposited at 620°C or 520°C by LPCVD using a SiH_4 source. Electron-beam evaporation in a UHV chamber and subsequent annealing in N_2 atmosphere were also used to obtain large-grain films. Gate oxides below 25 nm thick were deposited by LPCVD.

The variation of the drain current over time was directly measured using mercury batteries and an xy-recorder (Hitachi-4005). The response time of a recorder was 400 ms. The noise power spectrum was measured using low-noise amplifiers and an HP 3585A spectrum analyzer.

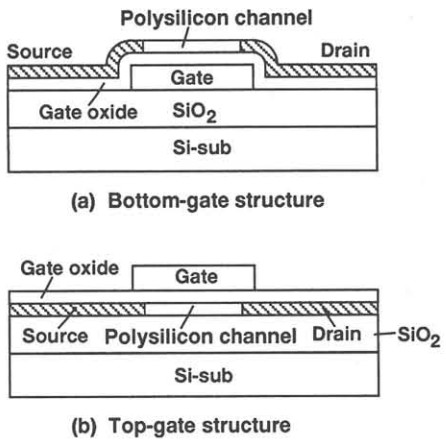

Fig. 2 Schematic cross-sectional structures of (a) bottom-gate and (b) top-gate polysilicon TFTs.

3. RESULTS AND STABILITY ANALYSIS

The variation of the drain current over time, measured for p-channel top-gate TFTs with a drain voltage of -3 V, is shown in Fig. 3. Drain current fluctuations δid in the TFTs are found to be considerably larger than those in single-crystalline-Si (bulk-Si) MOS transistors in spite of the smaller transconductances.

Since the origin of this large 1/f noise is attributed to the fluctuation in the number of trapped carriers δnt in the CVD gate oxides, that is, the fluctuation in the input side, the equivalent gate input voltage fluctuations $\delta v g$ corresponding to δid are used in our stability analysis. The δvg is given by $\delta vg = \delta id \cdot / gm$ (gm: transconductance). The noise power spectra over equivalent gate input voltage fluctuations, Svg, measured for both p-channel and n-

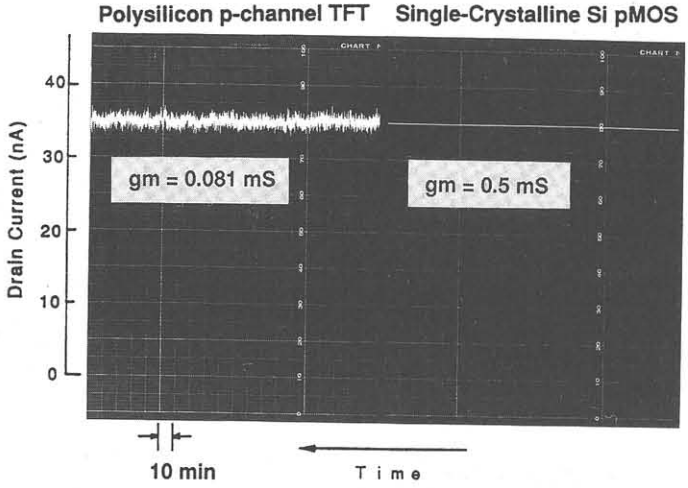

Fig. 3 Drain current fluctuation over time in polysilicon TFT and single-crystalline pMOS transistor. Vd = -3 V. Gate length and width are 1.2 and 0.6 μm, respectively, for both samples. Polysilicon channel films 38 nm thick were deposited at 620°C.

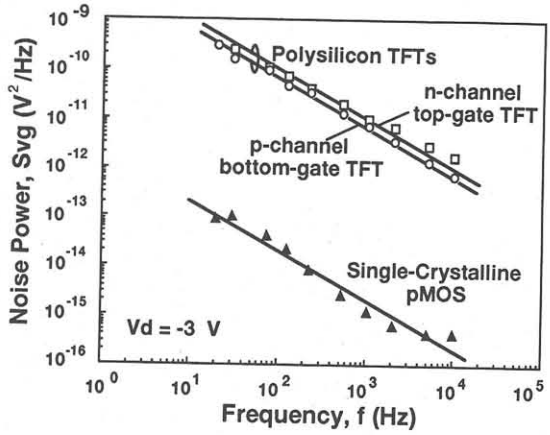

Fig. 4 Noise power spectra over equivalent gate input voltage fluctuations for polysilicon TFTs and single-crystalline devices.

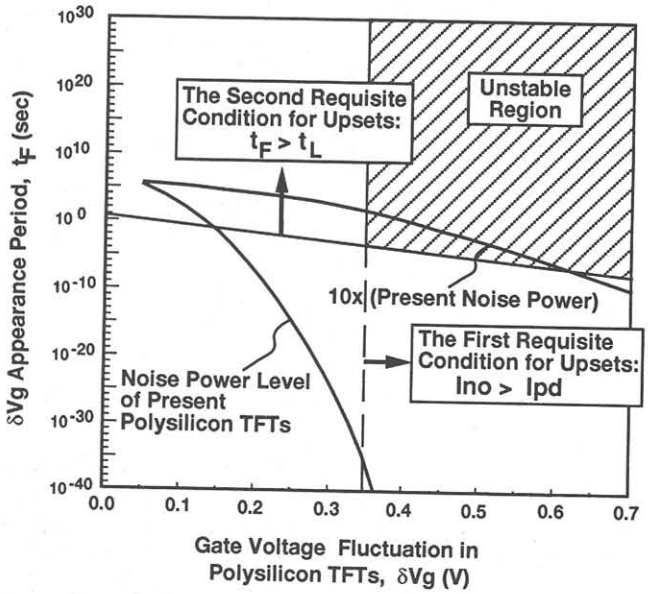

Fig. 5 Appearance period of the equivalent gate input voltage fluctuation in polysilicon TFTs and the unstable region of the cell. Retention mode with Vcc of 2 V is assumed. Total observation time is 280 hours.

channel TFTs are shown in Fig. 4, in comparison with bulk-Si devices. The noise values were normalized to those of the same size devices with a gate length and width of 1 μm, and a gate oxide thickness of 1 nm. The noise power spectra of TFTs are found to be about 10^4 times larger than those of bulk-Si devices.

The effects that gate voltage fluctuations in TFTs have on cell stability in the retention mode are examined here. The supply voltage Vcc and the high node voltage are 2 V. The positive gate voltage fluctuation δvg reduces the on-current of the p-channel TFT load, Ipd, and increases the off-current of the driver nMOS transistor, Ino. Next two requisite conditions have to be fulfilled for memory upsets. As the first condition, if Ino exceeds Ipd, the memory charge at the storage node can flow out through the driver transistor and the high node voltage cannot be sustained. In addition to this requisite condition, if the appearance time of the large gate voltage fluctuation, t_F, exceeds the discharge time of the memory charge, t_L, it is possible to lose the memory charge and stored information, thus causing memory upsets.

That is, the first requisite condition in our model for upsets: Ino > Ipd is given by

$$\delta vg > \frac{\alpha_n \alpha_p}{\alpha_n + \alpha_p} \log \frac{Ipd(\delta vg=0)}{Ino(\delta vg=0)} \qquad (1)$$

where αn and αp are subthreshold swings of driver nMOS transistors and p-channel TFTs, respectively. Ipd (δvg=0) and Ino (δvg=0) are the TFT on-current and nMOS off-current without gate voltage fluctuation.

The second requisite condition for upsets: $t_F > t_L$, is given by

$$tF > \frac{Vcc \cdot Cs}{Ino(\delta vg=0) \cdot 10^{\delta vg/\alpha n}} \qquad (2)$$

where Cs is the storage node capacitance. The unstable region satisfying above two conditions is shown in Fig. 5. Here, αn, αp, Ipd (δvg=0) and Ino (δvg=0) are assumed to be 80 mV, 500 mV, 0.1 nA and 1 fA, respectively. It is found that the gate voltage fluctuation over 0.35 V is required for memory upsets.

To clarify the effects of noise on the cell stabilty, we calculated the δvg appearance time, t_F, assuming that δvg fluctuates according to a Gaussian distribution. The probability that δvg results in a range between δvg and δvg + Δδvg is given by

$$P(\delta vg) = \frac{1}{\sqrt{(2\pi\overline{\delta vg^2})}} \exp(-\delta vg^2/2\overline{\delta vg^2})\,\Delta\delta vg \qquad (3)$$

$$\overline{\delta vg^2} = \int_{f1}^{f2} Svg\, df\, df \qquad (4)$$

where Svg is the measured noise power spectrum for δvg, and f1 and f2 are the lower and upper limits of a frequency band which are determined by the observation time and the response time of measurement, respectively. Using the P(δvg), the time t_F is given by $t_F = P(\delta vg)\cdot T$ (T:observation time). The calculated values of t_F are shown in Fig. 5, in comparison with the unstable region, for the noise power level of present polysilicon TFTs and a noise level 10 times larger. The total observation time T is 280 hours. We confirmed that the present noise level does not cause memory upsets and has a safety margin of about 10 times compared with the level in the unstable region. The most sensitive parameter defining the unstable region is the on-current Ipd of the TFT load. As shown in Fig. 6, a reduction in Ipd decreases the critical value of gate voltage fluctuation, δvgc, where Ino is equal to Ipd, rapidly enlarging the unstable region. Results demonstrate the importance of maintaining the TFT on-current.

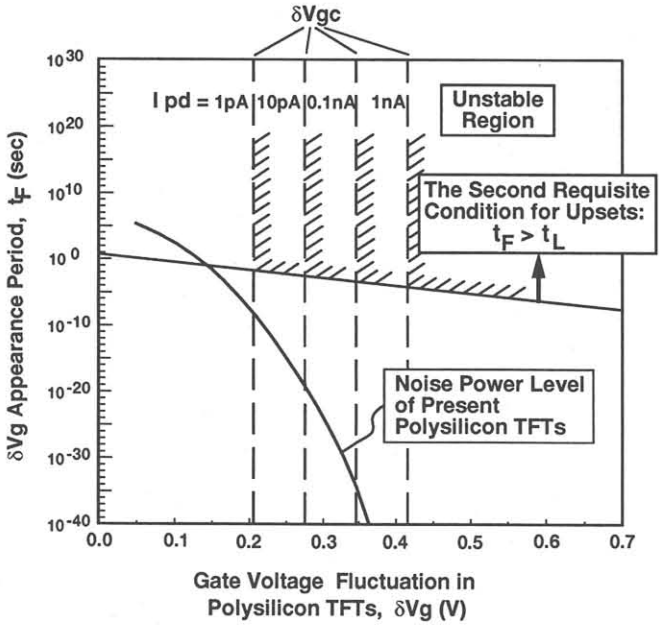

Fig. 6 TFT on-current dependence of the unstable region. Vcc = 2 V, Ino = 1 fA, αn = 80 mV, αp = 500 mV.

Although large 1/f noise in TFTs is firstly caused by high trap densities in gate oxides, it is strongly correlated with the potential barrier height at the grain boundary in a polysilicon channel, particularly at low current levels, as shown in Fig. 7. The fluctuations in the number of trapped carriers in oxides, δnt, cause not only fluctuations in the number of conduction carriers δn, but also large activated-mobility fluctuations δμ, at low current levels. This is because the barrier height fluctuates by δnt. Thus, the barrier lowering was also found to be very effective in reducing noise.

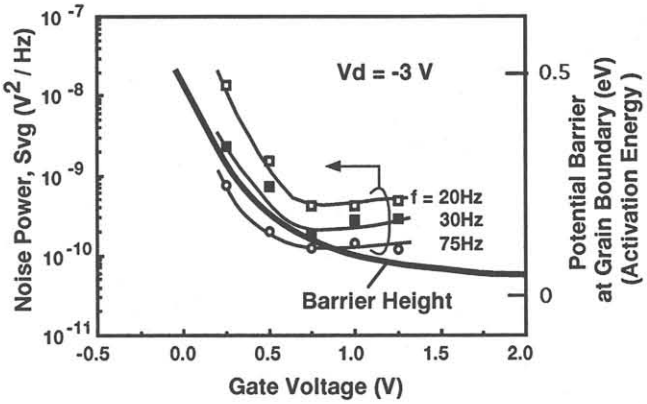

Fig. 7 Noise power spectra of equivalent gate-input-voltage fluctuations and potential barrier at grain boundary(activation energy) in top-gate n-channel TFTs. The polysilicon channel layer with thickness of 200 nm was deposited using EB evaporation. Gate length and width are 1.2 and 100 μm, respectively.

4. CONCLUSION

We have observed very large drain current fluctuations over time in polysilicon TFTs. Assuming that equivalent gate voltage fluctuations have a Gaussian distribution, the effects of noise and a design principle for cell stability have been demonstrated. On-current improvement and lowering of the grain-boundary barrier were found to be essential to increase stability.

ACKNOWLEDGMENT

The authors wish to express their appreciation to M. Tsunematsu, K. Nagasawa, T. Matsumoto, S. Ikeda, T. Nishida of Semiconductor and Integrated Circuits Division, and Dr. M. Nagata, K. Sasaki, Dr. K. Ishibashi, Dr. Y. Kamigaki of CRL, for valuable discussions and experments.

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