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A Novel Technique for Investigating Hot-Electron-Induced Oxide Damages and Device Degradations in Submicron LDD n-MOSFET's

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In this paper, we developed a new characterizing method to extract the spatial distribution of interface states using charge pumping (CP) measurement and the time-dependent power-law relationship. Unlike other reported methods by adjusting the reversed drain bias, this method can profile the generated interface states ΔN_{it} as well as the effective time evolution of damaged length L_{dam}. By combining the characterized L_{dam} and ΔN_{it} quantitatively, consistent results can be reached that the damage at $V_{GS} = V_{DS}/2$ is most highly localized among the various stress biases, which can explain why the interface state is most responsible for the device degradation under long-term operating conditions at this bias.

1. Introduction

One of the most important reliability issue in submicron or deep-submicron MOS devices is the hot-carrier-induced oxide damages which results in the degradations of drain current, transconductance and threshold voltage shift[1]. These types of degradations in LDD n-MOSFET's are mainly attributed to the creation of interface states ΔN_{it} at the Si-SiO_2 boundary. So far, most of the studies are paid on the individual study of ΔN_{it} characterization[2-4] and its correlation with the aforementioned degradations[5]. Quite few[6] are focused on the correlation between ΔN_{it}, L_{dam} and the stress bias. In this paper, we have developed a new characterizing method to extract the spatial distribution of interface states using charge pumping (CP) measurement and the time-dependent power-law relationship. Unlike other existing methods by adjusting the reversed drain bias, this method can directly profile the generated interface states as well as the effective time-dependent damaged length. For demonstration, this paper begins with the implementing details of this technique, along with some illustrative results. Next, this newly-developed method is applied to LDD n-MOSFET's stressed at different biases so as to further investigate the device drain current degradation and its correlation with the oxide damages under long-term operating conditions.

2. Theory and Experiment

The LDD n-MOSFET's used in this study were 0.72-μm mask gate length, 20-μm channel width, 140-Å oxide thickness and 0.15-μm sidewall oxide spacer. Based on the power-law relationship[1,7], the increase of the maximum CP current $\Delta I_{cp,max}$ can be expressed as

$$\Delta I_{cp,max}(t) = C\left[t\,\frac{I_{DS}}{W}\,e^{-\phi_{it}/q\lambda E_m}\right]^{n(t)}. \qquad (1)$$

E_m is the maximum lateral channel electric field, q is the electronic charge, I_{DS} is the device drain current, W is the gate width, C is a proportional constant, λ is the carrier mean free path, $n(t)$ indicates the power-law dependence on stress time t and ϕ_{it} is a critical energy that a carrier must have in order to create interface traps. The values for these parameters are ϕ_{it} = 3.7 eV and λ = 67 Å. For simplicity, we assume that the lateral electric field distribution and drain current do not vary significantly over stress time. As described by Ancona *et al.*[6], in MOS devices with very thin gate oxides, the hot-carrier-induced interface state generation occurs in a relatively narrow zone (i.e., highly localized) and the peak is found to be well correlated with the location, where the lateral electric field reaches its maximum value. With this in mind, this highly localized interface state $\Delta N_{it}(x)$ can be approximated by a rectangular distribution in terms of a full width at half-maximum (FWHM) as in Fig. 1. The approximate ΔN_{it} profile has the non-zero value as

$$\Delta N_{it}(t) = \frac{\Delta I_{cp,max}(t)}{qWfL_{dam}(t)} \qquad (2)$$

only in the effective damaged region. f is the applied gate pulse frequency in CP measurement. $L_{dam}(t)$ for (2) can be derived as follows. First, keeping the definition of FWHM in mind and referring again to the power-law expression, we can get

$$\frac{\Delta N_{it,1/2}(t)}{\Delta N_{it,m}(t)} = \exp\left[\frac{n(t)\phi_{it}}{q\lambda}\left(-\frac{1}{E_{1/2}(t)} + \frac{1}{E_m}\right)\right] = \frac{1}{2}. \qquad (3)$$

Here, $\Delta N_{it,1/2}$ is defined as one half of the maximum interface state generation $\Delta N_{it,m}$ in tested device, and $E_{1/2}$ is the lateral electric field at a location where the induced amount of interface states is $\Delta N_{it,1/2}$. Next, we can rearrange (3) to solve $E_{1/2}$ as

$$E_{1/2}(t) = \left(\frac{1}{E_m} + \frac{q\lambda}{n(t)\phi_{it}} ln2\right)^{-1} . \quad (4)$$

As a consequence, the effective damaged length of the ΔN_{it} profile can be obtained by calculating the distance between the two $E_{1/2}$ locations.

3. Results and Discussions

Figure 2 shows the measured I_{cp} versus V_{gh} curves before and after various periods of channel-hot-carrier stress at V_{DS} = 7 V and V_{GS} = 6 V for this tested sample by using a fixed base level CP measurement[4]. In Fig. 3 we show the maxima (denoted by $\Delta I_{cp,max}$) of a sequence of such ΔI_{cp} curves plotted as a function of stress time in log-log scale. Initially, $\Delta I_{cp,max}$ increases largely with the increasing stress time, and then saturates. According to (1), the power-law index $n(t)$ can be extracted from the slope of the $\log(\Delta I_{cp,max})$ versus $\log(t)$ curve, as shown in Fig. 3. One important implication from Fig. 3 is that values of n varies with stress time, which is not a constant as one usually used.

Before determining the effective damaged length L_{dam}, in Fig. 1, the lateral electric field distribution was calculated by 2-D device simulation. Now, with this distribution, we can calculate $E_{1/2}$ (denoted in Fig. 1), as shown in Fig. 4, which decreases with the increasing stress time (i.e., with the decreasing power-law factor). Furthermore, the effective damaged length Ldam of the ΔN_{it} profile with a full width at half-maximum (FWHM) can be obtained from the distance between the two $E_{1/2}$ locations, as in Fig. 1. Given the $\Delta I_{cp,max}$ and L_{dam}, the induced ΔN_{it} distribution can thus be calculated from (2) as in Fig. 5. Since for LDD n-MOSFET's, the characterized oxide trapped charges Q_{ox} are less significant by comparing with the calculated ΔN_{it}[8], we also applied this method to tested devices under different bias conditions. From Figs. 6 and 7, we can see that the effective damaged length is the shortest at V_{DS} = 7 V and V_{GS} = 3 V (or $V_{GS} = V_{DS}/2$),which in turn leads to the rapid increase of interface traps with stress time (shown in Figs. 8 and 9) and so enhances the degradation of drain current (shown in Fig. 10). In other words, for the devices stressed at the maximum substrate current ($V_{GS} = V_{DS}/2$), the oxide damage has been mainly attributed to interface trap generation through carriers[3]. Fig. 11 shows the fitting parameters in L_{dam} and ΔN_{it} respectively with a power form under different bias conditions. It reveals that with increasing stress time, the quantity of ΔN_{it} at V_{GS} = 3 V is the largest finally. However, from the beginning of stress (Fig. 8), the quantity of ΔN_{it} is not the largest. It means that in judging the current degradation in n-MOS devices, the criteria should consider both the combined effects of ΔN_{it} and oxide damaged region length.

4. Conclusions

In this work, a new method has been developed for characterizing the time evolution of interface states in spatial distribution and the oxide damaged region. It is worthwhile to note that this newly-developed method significantly eliminates the repetitive CP measurements, and hence avoids the likely imposition of re-stress on tested devices. Device drain current degradation can be well and accurately described by way of generated interface state and the damaged region length. This method is easy-to-implement and is also a good and precise monitor of the hot carrier reliability in VLSI/ULSI device design.

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References

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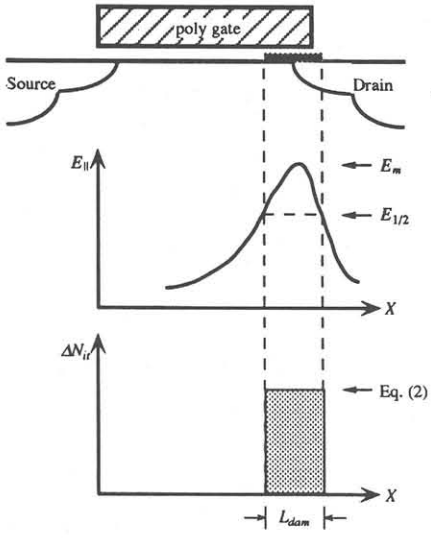

Fig. 1 Schematic illustration of the new profiling technique. The oxide damaged region along with the lateral electric field, is also shown.

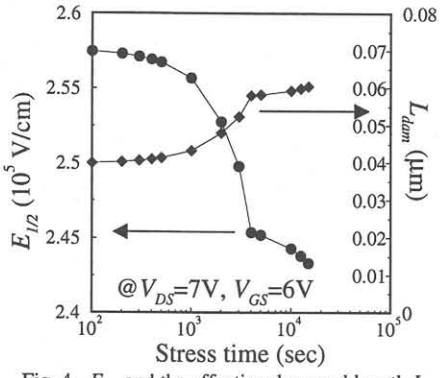

Fig. 4 $E_{1/2}$ and the effective damaged length L_{dam} versus time.

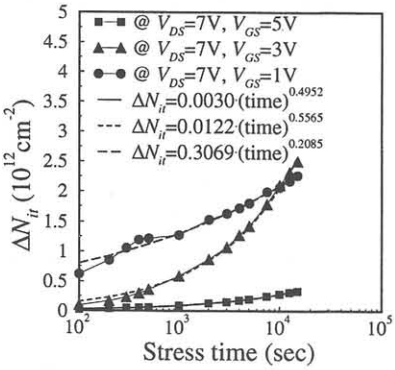

Fig. 8 Time evolution of $\Delta N_{it}(x)$ at various stress biases.

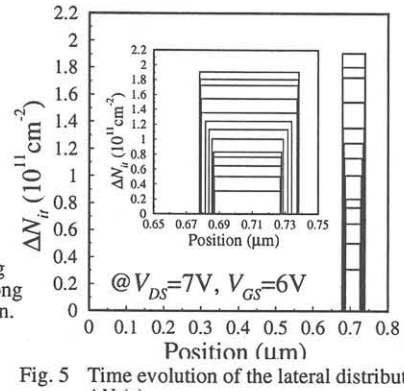

Fig. 5 Time evolution of the lateral distributions of $\Delta N_{it}(x)$.

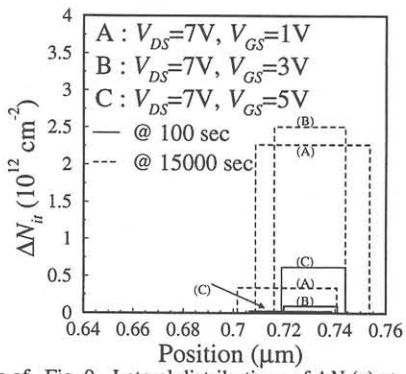

Fig. 9 Lateral distributions of $\Delta N_{it}(x)$ at various stress biases for 100 and 15000 sec.

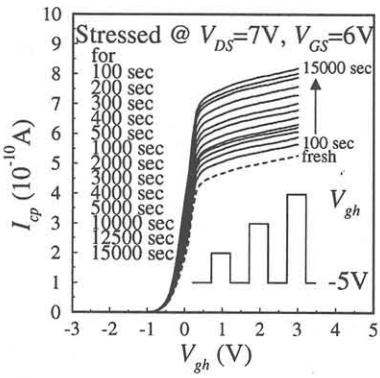

Fig. 2 Measured I_{cp} versus V_{gh} curves before and after various time stress. Frequency is 1 MHz.

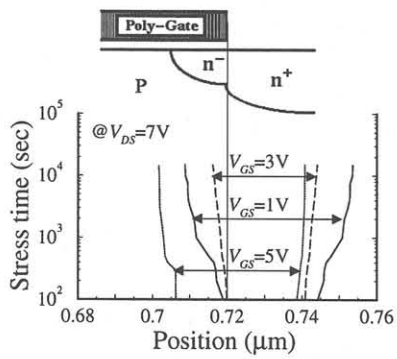

Fig. 6 Comparison of damaged regions for devices at different stress biases.

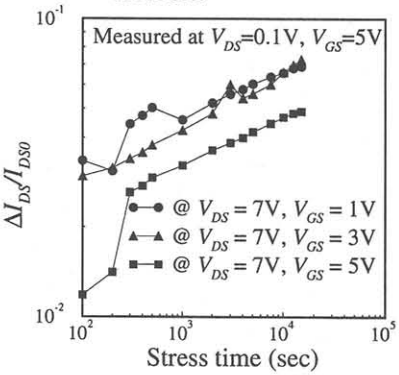

Fig. 10 $\Delta I_{DS}/I_{DS0}$ versus time at various stress biases for comparison.

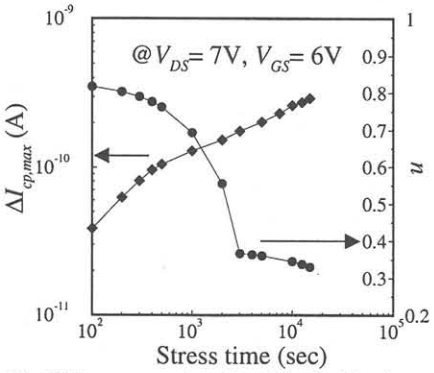

Fig. 3 $\Delta I_{cp,max}$ versus time from Fig. 2. The time-dependent power law index n is shown on the right.

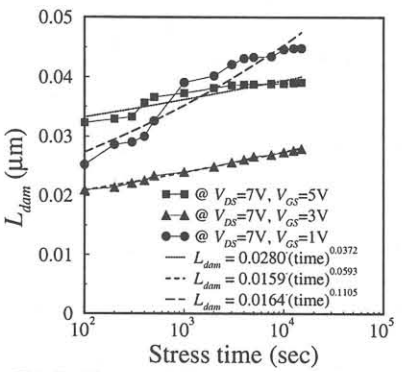

Fig. 7 Time evolution of the damaged region length at various stress biases.

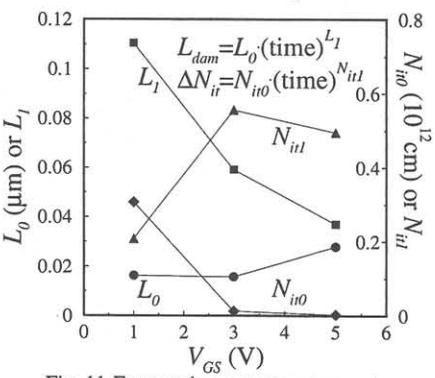

Fig. 11 Extracted parameters versus stress gate biases for Figs. 7 and 8.