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Ultra Shallow p+n Junction Formation Using the Solid Phase Diffusion(SPD) through 'a-Si/Thin Barrier Oxide' Layer

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A new process technology was described in order to obtain the ultra shallow p^+n junction. For this purpose, we have tried to drive-in the solid source of B_2O_3 through 'amorphous Si / thin barrier oxide' layer. The deposited amorphous Si layer is fully converted into an oxide layer during wet oxidation. This oxide layer was used as a side-wall in MOSFET structure through RIE. Using this process, we have obtained the junction depth of about 30nm with 3×10^{19} cm^{-3} surface concentration.

1. Introduction

In order to reduce the punchthrough phenomena which is one of the limiting factors in the scaling-down of MOS transistor, the junction depth of source/drain should be as shallow as possible. The purpose of this study is to develop the shallow p^+n junction technology suitable for deep submicron PMOSFET, which is in the range less than 0.05μm.

For this purpose, we have tried to drive-in the solid source of B_2O_3 through 'amorphous Si(a-Si) / thin oxide' layer, where a-Si layer plays a role as a boron sorption layer and the thin oxide as a diffusion barrier and simultaneously piling-up of B atoms[1-3].

The commercialized B_2O_3 solid source wafers are well controlled to dirve in boron atoms into Si substrate and highly reproducible. This diffusion process has the advantages of a symmetric S/D doping in MOSFET, no damage, and no channeling in comparision with ion implantation method.

We have characterized the boron depth profiles by SIMS and fabricated a PMOSFET using this process.

2. Experimentals

The starting substrate was n-type, (100) Si wafers with a resistivity of 10~15 Ω-cm. First, thin oxide layer was thermally grown 7nm or 9nm in dry oxygen ambient at 850°C. This thin oxide layer is utilized as a diffusion barrier and piling-up layer for boron atoms. Subsequently, amorphous Si layer was deposited 45nm by LPCVD at 560°C. And, boron atoms were diffused into the 'amorphous Si / thin barrier oxide' layer from B_2O_3 solid source wafers. As a result, boron tail region is formed within Si substrate with a considerably high surface concentration and ultra shallow junction depth.

Then, the deposited a-Si layer is fully converted into an oxide layer during wet oxidation. We have obtained SIMS depth profiles and applied this process for the fabrication of PMOSFET.

3. Results and Discussions

Fig.1 shows the sheet resistance variations with diffusion temperature in the solid phase diffusion(SPD) into single crystal Si from the B_2O_3

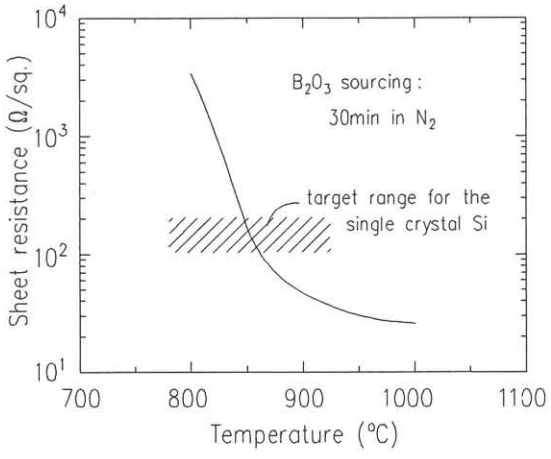

Fig.1 Sheet resistance variations with drive-in temperature in the solid phase diffusion(SPD) into the single crystal Si substrate.

solid source, which is performed to obtain the proper diffusion conditions. In all cases, the diffusion time was fixed at 30min. As a result, we selected the dashed area as the proper conditions.

Fig.2 shows the SIMS depth profiles of the boron atoms drived into 'a-Si / thin oxide / Si sub.' samples, in which the SPD was performed for 30min at 850° C. The thin oxide was grown by thermal oxidation(profiles a, b) in a pure oxygen furnace or by the boiling in H_2SO_4 solution for 10min at 120°C(profile c) before the deposition of a-Si of 450Å. In profile 'd', any native oxide was removed just before a-Si deposition. We can see that the 'a-Si / Si sub.' interface with or without a thin oxide layer plays a role of the diffusion barrier and the piling-up of borons. The B-sorbed a-Si layer(450Å) was converted into an oxide layer(about 1000Å) during wet oxidation for 30min at 850° C and used as a side-wall oxide in the gate structure of MOSFET through RIE process.

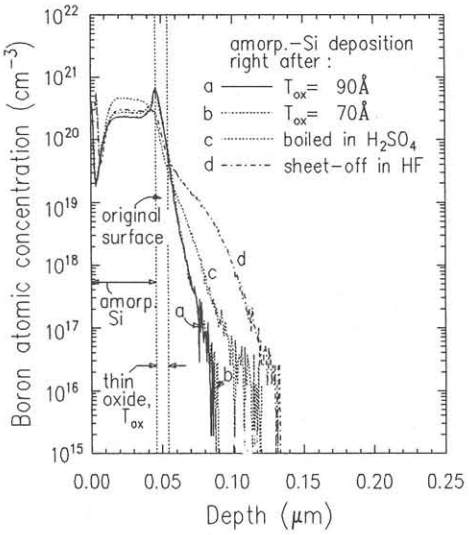

Fig.2 SIMS depth profiles of the boron atoms diffused into Si substrate through 'a-Si / thin oxide' layer from B_2O_3 solid source.

Fig.3 shows SIMS profiles of the boron atoms redistributed during the wet oxidation of amorphous Si layer. As shown in the figure, we can see that the redistribution within Si substrate was not occurred during wet oxidation. The junction depth in profiles 'a' and 'b' was about 30nm and the surface concentration was about $3\times10^{19}cm^{-3}$. From above results, we can expect that the SPD method into 'a-Si / thin oxide' layer from B_2O_3 solid source would be effectively applied to the formation of ultra shallow p^+n junction.

Table 1 shows the thickness of the oxide layers grown during wet oxidation in the samples of several conditions. As shown, the oxidation rate of the diffused a-Si layer(case A) was about 1.9 times higher than that of the bare Si(case D), which indicates that the selective oxidation of only a-Si layer can be easily controlled.

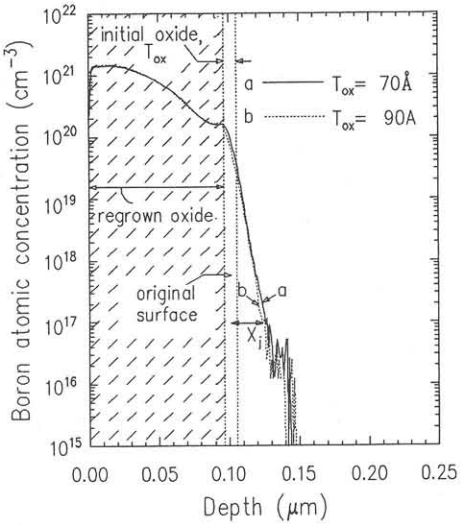

Fig.3 SIMS depth profiles of the boron atoms redistributed during wet oxidation of amorphous Si layer.

Table 1. Oxide thickness values after wet oxidation for several sample conditions.

Sample Condition before Oxidation	Oxide Thickness after Wet Oxidation(Å)
A : 'diffused a-Si / Si sub.'	1,034
B : 'a-Si / Si sub.'	814
C : 'diffused Si sub.'	634
D : 'bare Si'	545

The process schematics for the application of the SPD method to PMOSFET fabrication was shown in Fig.4. Gate oxide thickness was 8nm and the p^+ poly Si gate of 2500Å was defined with PSG (Phosphosilicate Glass) oxide of 6500Å. After thin oxidation, a-Si deposition, and B_2O_3 drive-in(Fig.4(a)), the B-doped a-Si layer was oxidized(Fig.4(b)). Through this technology, we could obtain a thermally grown side-wall oxide with the quality much better than any other(APCVD, TEOS, HTO, etc.). That is, the oxidized layer becomes a side-wall oxide by RIE process. And the p^+ layer formed by SPD is used as the ultra shallow junction under the side-wall oxide. In HF solution, PSG layer was removed much faster than thermal oxide, as shown in Fig.4(d). Finally, Ti deposition and silicidation was performed.

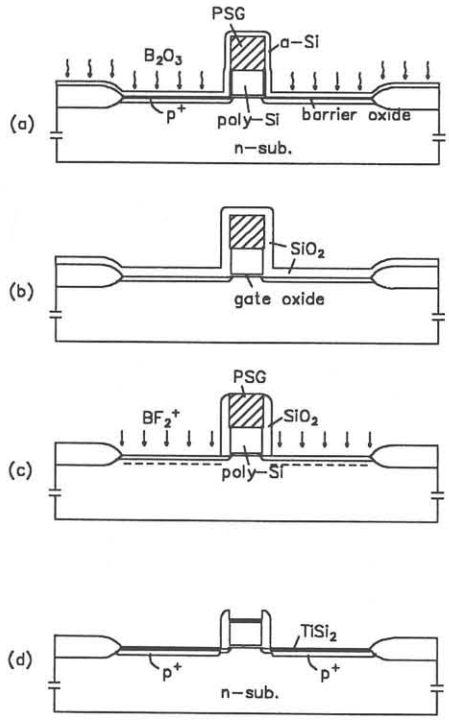

Fig.4 The process schematics for the application of SPD method to PMOSFET fabrication : (a) gate definition and SPD, (b) wet oxidation, (c) oxide RIE and BF_2^+ implantation, and (d) PSG wet etching and Ti silicidation.

Fig.5 shows the SEM cross section of the gate structure formed according to above procedures. Drain current and voltage characteristics of a fabricated PMOSFET is shown in Fig.6, of which gate length is about 0.76μm.

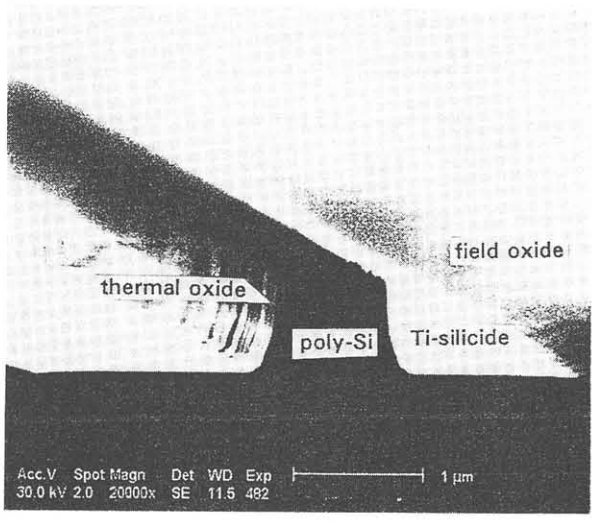

Fig.5 SEM cross section of the gate structure with a thermal side-wall oxide.

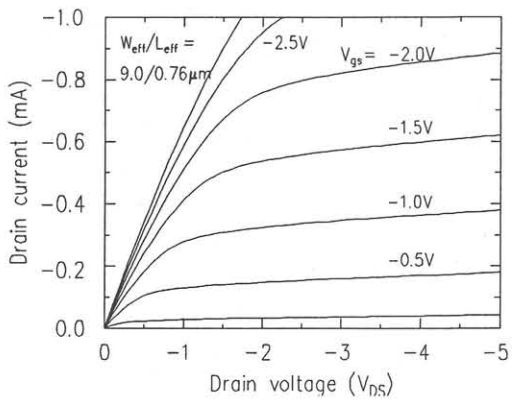

Fig.6 I_d-V_d characteristics of the PMOSFET fabricated using the SPD method. Effective channel lengh and width were 0.76μm and 9.0μm, respectively.

From above results, we can confirm that the SPD method is practicable for the fabrication of deep-submicron PMOSFET.

4. Conclusions

We have developed a new processing method fabricating the ultra shallow p^+n junction, in which boron atoms are drived from B_2O_3 solid source through 'a-Si / thin oxide' layer. In this case, the thin oxide have a good role as a diffusion barrier and piling-up layer for boron atoms. Using this process, we could obtained the junction depth of about 30nm with surface concentration of 3×10^{-19} cm^{-3}.

Acknowledgment

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References

[1] K. Park, S. Batra, S. Banerjee, G. Lux, and R. Manukonda, MRS Symp., 182(1990) 141.

[2] I. R. C. Post and P. Ashburn, IEEE Trans. ED, 38(1991) 2442.

[3] K. Suzuki, Y. Yamashita, Y. Katkoka, K. Yamazaki, and K. Kawamura, J. Electrochem. Soc., 140(1883) 2960.