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On the Use of Indium and Gallium as P-Type Dopants in Si 0.1 μm MOSFETs

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We fabricated 0.1 µm devices employing In and B as a p-type channel dopants [1] to investigate the short channel effect. In this report, we investigate the advantages of using In in comparison to B with respect to gate quality, mobility and threshold voltage. It is concluded that the use of In shows no direct disadvantages. The advantage of using In lies in the suppression of the short channel effect. The conventional planar bulk device can be scaled further at least for one generation of MOS transistors without loss in current driveability. Secondly, the feasibility of Ga as a p-type extension is investigated.

1. Introduction

Indium and Gallium have been studied in the past for possible use in Si MOSFET technology. Although both dopants were considered to be disadvantages because of their low solid solubility, recently a new interest arose in using Indium for the channel implantation. In the past few years a lot of effort was devoted to solve the problems in scaling down the silicon MOSFET to the 0.1 µm region. Several publications [2,3] have shown that the planar bulk technology with a careful S/D and channel engineering is a good candidate for ULSI systems. Especially the implementation of shallow extensions and the Ground Plane (GP) concept are effective in suppressing the short channel effect (SCE) [4,5] while keeping a high current drive. They reduce the SCE by restoring the 1D potential profile under the gate as shown in Fig.1.

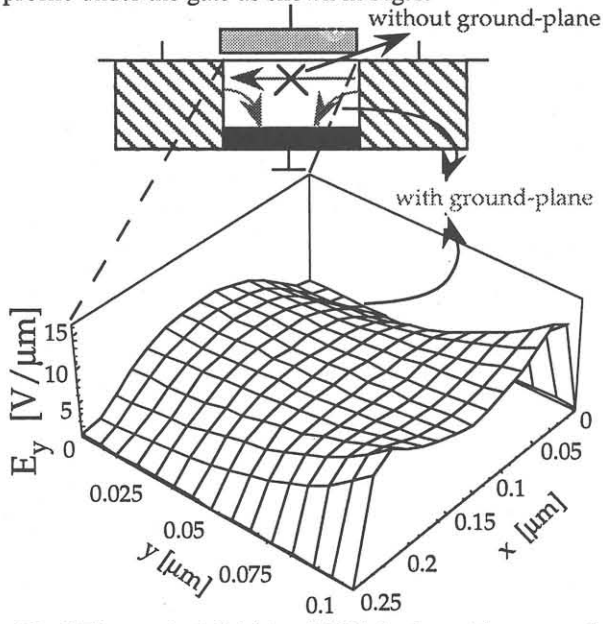

Fig.1 The vertical field in a MOS device with a ground plane shows two bumps which indicates a restoration of the 1D potential profile under the gate

It is indeed preferable to have a way to pull down the channel fields because that prevents the lateral drain field to penetrate through the channel into the source which lowers the barrier against diffusion (DIBL). The use of Indium as a channel profile to mimic the GP concept in nMOSTs has been shown several times [1,2,3]. The use of Gallium as an extension in pMOSTs will be suggested.

2. Indium as a p-type channel profile

Indium as a p-type dopant in Si has been used and studied in the past for IR detectors [6]. Antoniadis [7] argued on the basis of a strong oxidation enhanced diffusivity and a rapid outdiffusion through the SiO_2 that In is not a viable alternative to B as a field region implant in a CMOS technology. Recently, the use of In to form a ground plane in the channel region has been proved by fabricating devices. However, a more fundamental study on the impact of In concerning the behaviour of the nMOST has not been reported yet.
In our nMOS run [1], we fabricated capacitors with an area of 14529 μm^2 and perimeter of 508 µm on (100) Si implanted with In (1E13 cm^{-2}, 190 KeV) or B (1.5E13 cm^{-2}, 35 KeV) respectively. The gate oxide thickness grown at 800°C is 5.6 nm. All wafers were oxidised together in the same furnace. Fig.2 shows the tunnelling characteristics for both dopants, *showing clearly a higher breakdown field in case of In.*

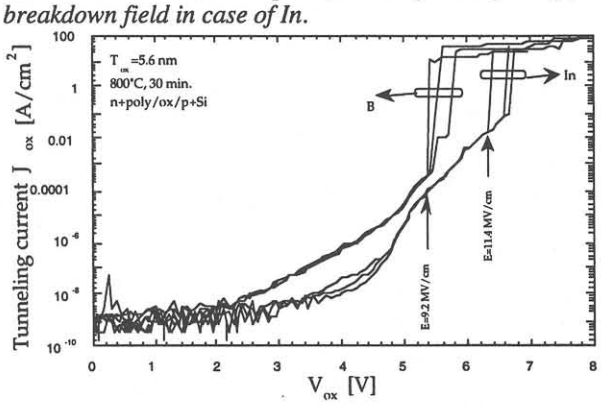

Fig.2 Tunnel currents through thin gate oxide showing breakdown characteristics

Fig.3 plots the effective mobility of In and B transistors against an effective field $E_{eff}=(0.5\ Q_{inv}+Q_{bulk})/\varepsilon_{si}$ for different bulk-source voltages. For high E_{eff}, a universal

mobility curve [8] is obtained. For lower fields, the non-universal roll-off is observed because of the oxide charges (Q_{ox}=1E11 cm^{-2}) present [9] which increase the Coulomb scattering. From this graph can be concluded that *In can safely replace B in the channel region without any loss of current drive.*

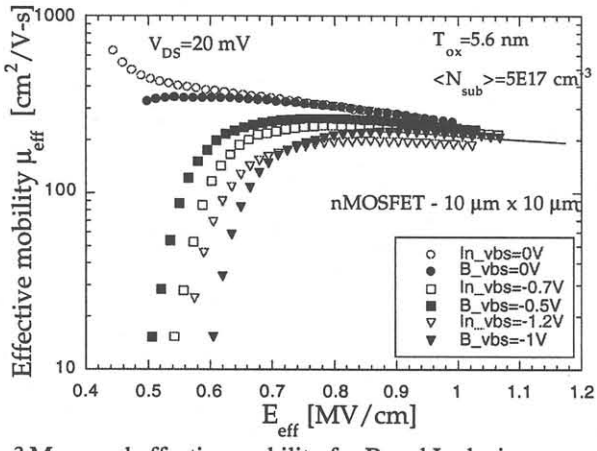

Fig.3 Measured effective mobility for B and In devices

For the low field bulk mobility of holes, we performed a Hall-measurement of an In implanted n-type Si wafer (10^{15} cm^{-3}). The insert of Fig.4 shows the spreading resistance measurement (SRP) of the sample. We plotted the measured bulk mobility in Fig.4 and compared with the mobility curve of B [10]. Despite the fact that In is a bigger atom, it seems *to provide nearly equally mobile holes as B does.*

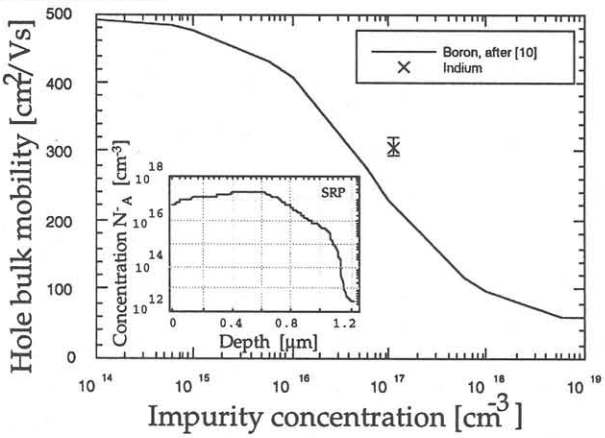

Fig.4 Low field bulk mobility for B and In in Si. The insert shows the SRP profile of the measured sample

A particular concern is the electrical activation of the In dopants. The activation energies (E_A-E_V [eV]) for the p-type dopants are 0.046 eV (B), 0.065 eV (Ga) and 0.16 eV (In). It is apparent that In has is a rather deep acceptor with a large activation energy which might lead to an incomplete ionisation of the dopant ensemble. The number of ionised dopants N^-_A can be calculated as given by [11]

$$N_A^- = \frac{P_\xi}{2}\left(\sqrt{1+\frac{4N_A}{P_\xi}}-1\right) \quad with \quad P_\xi = \frac{N_V}{g_A}exp\left(\frac{E_V-E_A}{kT}\right)$$

with N_A the total number of substitutional dopants and g_A the degeneracy factor (g_A=4).

In Fig.5, we plotted $f^-=N^-_A/N_A$, the ionisation factor, versus N_A. One can see that for N_A=1E18 cm^{-3} only 10% is ionised which can apparently contribute to the V_T and the 'ground plane'-action to reduce the SCE. To verify this we carried out an SRP and a SIMS measurement on an annealed Si sample implanted with In.

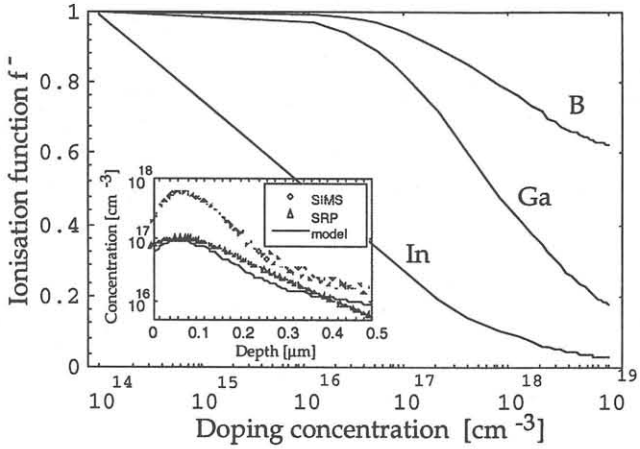

Fig.5 Ionisation function for three p-type dopants. The insert shows measured profiles to verify the model

The insert of Fig.5 compares this SRP and SIMS as well as the model for N^-_A (using the SIMS results as N_A), clearly showing an inadequate ionisation (the peak concentration is reduced by a factor of 7). In this analysis, the ionisation energy E_A was considered to be constant. It has been experimentally observed for B that E_A-E_V decreases with concentration for N_A>1E18 cm^{-3} [12]. For In, such a decrease is present but less pronounced because of its low solubility. In the model we compensated this by using g_A=1.

However, one important issue we left out so far is the fact that in a MOSFET the value of E_A-E_F or consequently the number free carriers is modulated by the gate electrode. The modulation makes E_A-E_F negative and the exponential in the Fermi-Dirac statistic for the dopants becomes nearly equal to zero resulting in an N^-_A approaching N_A [7] and f^- approaching 1. We investigated the exact influence of the gate on the degree of ionisation by using the 2D simulator MEDICI to calculate the V_T. We plotted in Fig.6 the number of holes (N_{h+}) and electrons (N_{e-}) for E_A-E_F=0 eV (~B) and for E_A-E_F=160 mV (In), together with the chemical concentration N_A. A remarkable difference in N_{h+} for B and In is observed. The N_{e-} in case of In is a factor of 3 higher at the surface.

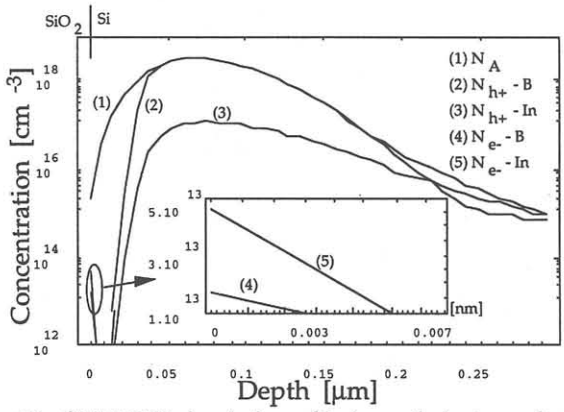

Fig.6 MEDICI simulation of holes and electrons for a given channel profile N_A being B or In

Fig.7 shows the resulting electrical potential for both cases. One can observe an increased surface potential of about 35 mV for the In, which leads to a reduction of V_T by the same amount, or for a targeted V_T of 0.4 V that is less then 10% which can easily be accounted for. Therefore, *the fact that In is a deep level impurity does not pose a serious problem for the V_T control.*

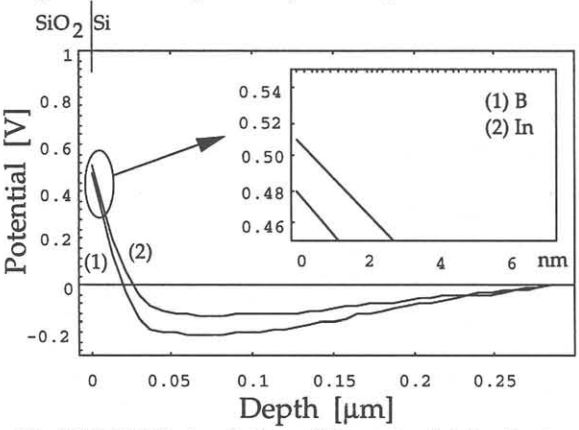

Fig.7 MEDICI simulation of the potential for the two cases (B and In) of Fig.6

3. Gallium as a p-type extension

Gallium as a p-dopant in Si has been studied and used in the past for the fabrication of thyristors. It had relatively little importance in CMOS because Ga has a rather low solubility in Si (2E19 cm^{-3} at 1000°C) [13] and is not masked by SiO_2. The diffusion in SiO_2 was investigated in [14] and it was concluded that the anneal in an ambient which contains traces of H_2 significantly increases the diffusion. Further, a considerable amount of dopants gets evaporated except when capped by a Si_3N_4 layer. As such, in a modern planar 0.1 μm CMOS process with a reduced overall temperature budget, clean processing and nitride spacers, *Ga might again be considered for ultra shallow extensions* ($N_{ext} \leq 2e19$ cm^{-3}). Because of its higher mass compared to B, it gives shallower implanted profiles and thus shallower extensions.

A concern with Ga is the evaporation from the Si lattice. Fig.8 shows the results of an experiment where we annealed for 40 min. in N_2 to see the evaporation from the Si substrate covered by a 10 nm thermal implantation oxide. We find an activation energy of only 0.32 eV in Si compared to 0.75 eV in SiO_2 [14] for an uncapped sample. This indicates that the use of a Si_3N_4 capping layer is necessary to minimise this evaporation. Experimental results will be presented on the conference.

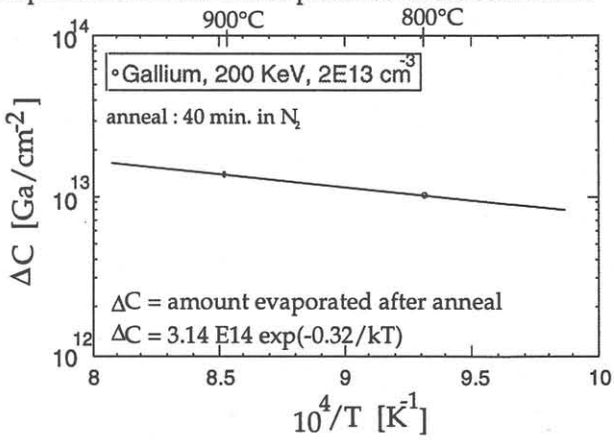

Fig.8 Arrhenius plot of evaporation ΔC for Ga in Si

4. Conclusion

We investigated the advantages and disadvantages of In in comparison to B with respect to gate quality, mobility and threshold voltage. We concluded that the gate quality of In devices is as good or even better than of the B devices. Concerning the mobility, the much heavier element In seems to provide equally good mobility curves. Further, it was shown that, although In is a rather deep impurity level, its effect on the V_T is less than 35 mV. The feasibility of Ga as a p-type extension was investigated and it was concluded that Ga can only be used in a low temperature budget process with Si_3N_4 as spacer technology.

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