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Fabrication of a Si Nanometer Column pn Junction and Implanted Damage Evaluation by TEM

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Si nanometer structures are promising for exhibiting the quantum size effect at temperature even as high as a room temperature. The aim of the present work is to fabricate 1-D tunneling pn diode. We have fabricated Si nanometer columns by RIE and thinnning by oxidation, and evaluated and the damages induced by a heavy ion-implantatio to the fine Si columns. In the case of heavy doping of As as well as BF_2, typical damages such as dislocations, Si micro-crystals and twins are observed. However, it should be noted that no damage is observed for fine Si columns with diameters less than 20nm in the case of As doping . It is suggested that defects are diffused out to the surface for ultra fine Si columns during annealing.

1.Introduction

Si nanometer wire is one of the most promising structures which exhibit quantum size effect such as formation of one dimensional (1-D) sub bands, and band gap expansion [1]. Although there are many difficulties in fabricating 1-D Si nanometer quantum wires, we have found that anistropical dry etching of Si columns and a subsequent isotropical thinning by oxidation is an excellent method with a high reproducibility [2,3]. The aim of the present work is to fabricate 1-D pn junction which is embedded in a Si nanometer column (Fig.1), since there is a possibility of electron tunneling between 1-D sub bands across p and n regions . Asume that a depletion layer width is smaller than 10nm due to high impurity concentrations and several 1-D subbands are occupied. Tunneling of electrons between subbands in p and n regions occur when an applied DC voltage make their energy difference smaller than kT, and multiple peaks of negative resistance will be observed with changing the applied voltage as shown in Fig.2. In order to observe this effect, heavy doping of impurities must be necessary. The present work focuses on the fabrication of sub ten nanometer Si columns, and the evaluation of the ion implanted damages by heavy doping by TEM observations.

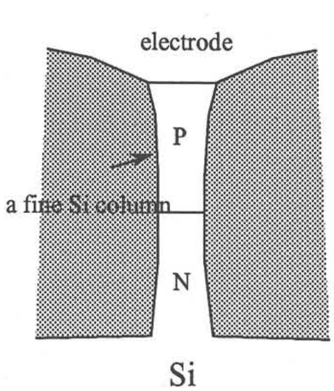

Fig.1 Schematic diagram of a Si nanometer column 1-D pn junction

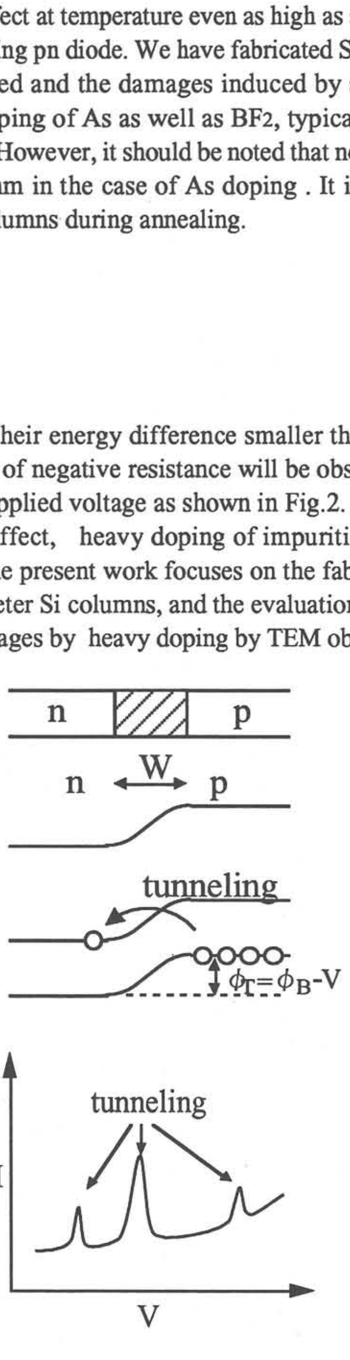

Fig.2 Estimated I-V characteristics of 1-D pn junction

2.Results and Discussions

At first fine dots patterns of resists (Shipley, SAL 601-ER7) were delineated by the electron beam lithography, and Si columns with diameter of 100 to 200 nm were formed by the anisotropic dry etching. Then Si columns were thinned further by the oxidation, and finally a few tens nanometer Si columns were fabricated(Fig.3).

Then As (arsenic), or BF_2 (boron-difluoride) were heavily ion implanted to the projection range of 20 to 40 nm, and these samples were annealed at 1000℃ for 30min in N_2 ambient. As implanted structures were amorphouos in both cases. In the case of BF_2 (30keV, $1x10^{16}cm^{-2}$), heavy damages such as dislocations and twins which occur at (111) planes were formed in 30nm Si columns (Fig.4). Several recrystalized Si layers are observed in the column. High magnification lattice image shows that the lattice plane spacing in this area is 3.13 Å which corresponds to {111} planes. Thus, these layers are twins as shown schematically in Fig.4. Formation of twins are typical in the case of solid phase epitaxial growth[4,5].

In the case of As (50keV, $4x10^{15}cm^{-2}$), as-implanted structure was amorphous, and dislocations with the Burgers vector of [111] direction were generated after annealing for the Si columns which diameter were larger than a few tens of nm, as shown in Fig.5.It should be noted that no damage was observed for the fine Si columns which diameter were less than 10nm. TEM lattice images of the ultra fine column which diameter is 8nm

is shown in Fig.6. It is shown that damage is completely recovered and an excellent crystalinity is obtained. It is suggested that diffusion lengths of defects at 1000℃, 30min are larger than the columns diameter and they are removed to the surface or the Si/SiO_2 interface during annealing.

It should be noted that damages such as dislocations were observed even in the region deeper than the ion projection range. It is considered that ions were implanted from both top and side walls. Thus, it is required to protect the side wall for fabrication of a less-damaged pn junction, and this is also effective to make an abrupt pn junction. An attempt to fabricate this is in progress by usage of organic SOG as an protection layer.

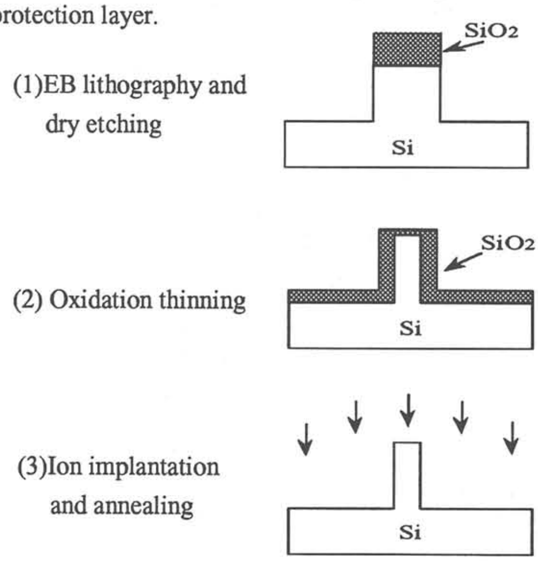

Fig.3 Fabrication procedure of a Si column

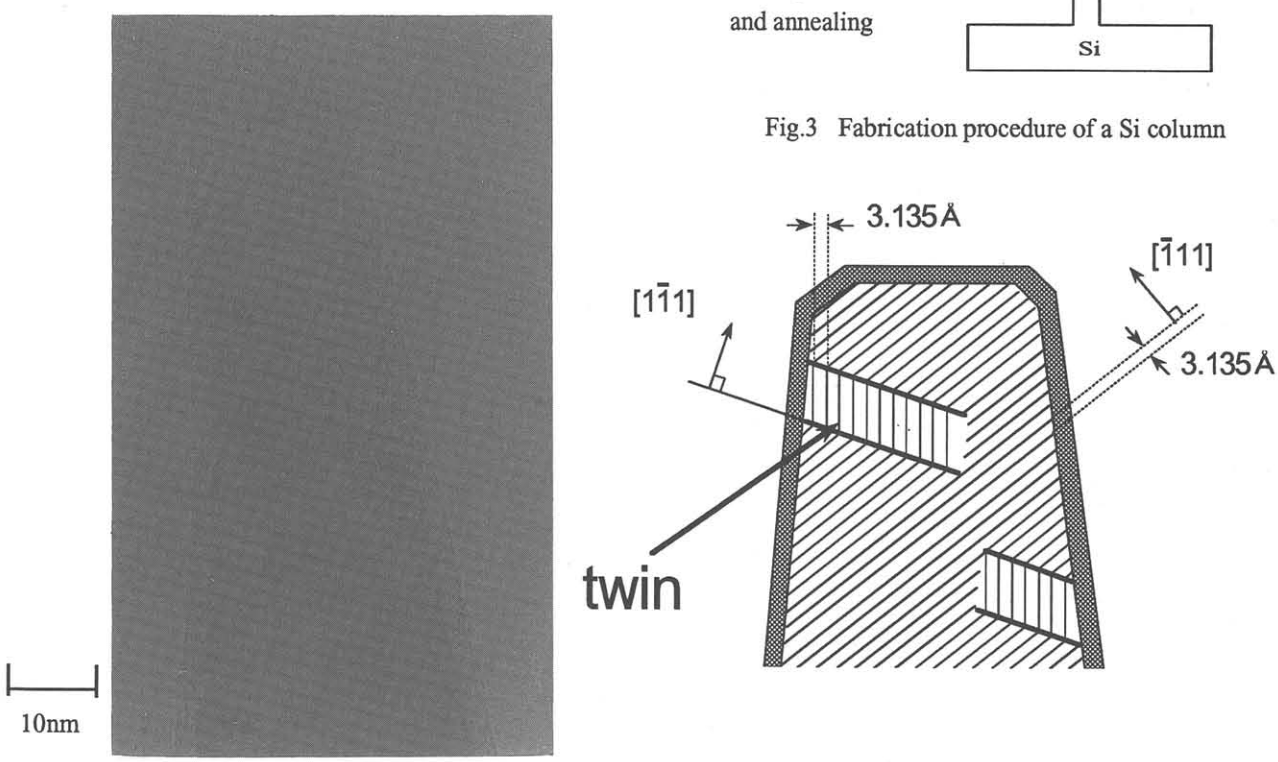

Fig.4 TEM micrograph of the 40nm Si column implanted by BF_2($1x10^{16}cm^{-2}$, 30keV) and annealed at 1000℃ for 30min. Twins and dislocations are formed.

3.Conclusion

Fabrication of the ultra fine Si column pn junction with the diameter of 8nm has been accomplished successfully. Damages such as dislocations and twins are observed by TEM for As and BF_2 implanted columns for which diameters are larger than 20 nm. It should be noted that the damages induced by the ion implantation are completely eliminated for the ultra fine Si columns which diameters are less than 10 nm, and it is considered that point defects and dislocations are annealed out to the surface by diffusion during annealing. It is strongly suggests that the damages induced by the heavy ion implantation can be removed easily especially when the Si column diameter is reduced below 10 nm. Electrical characterization of these ultra fine pn junction will made in near future

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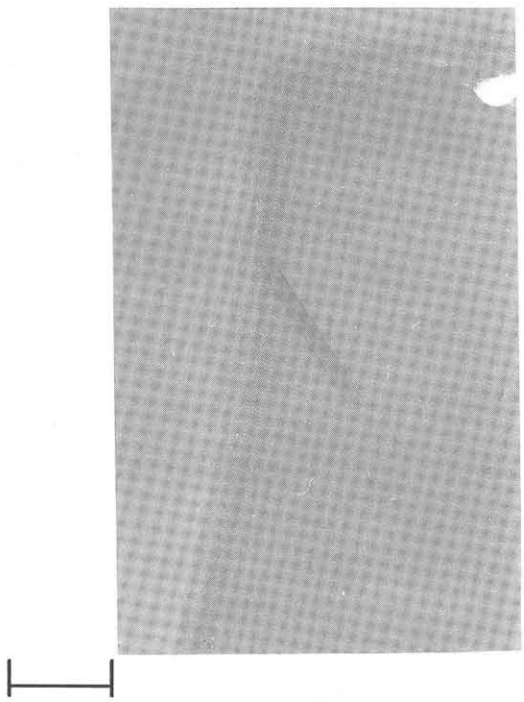
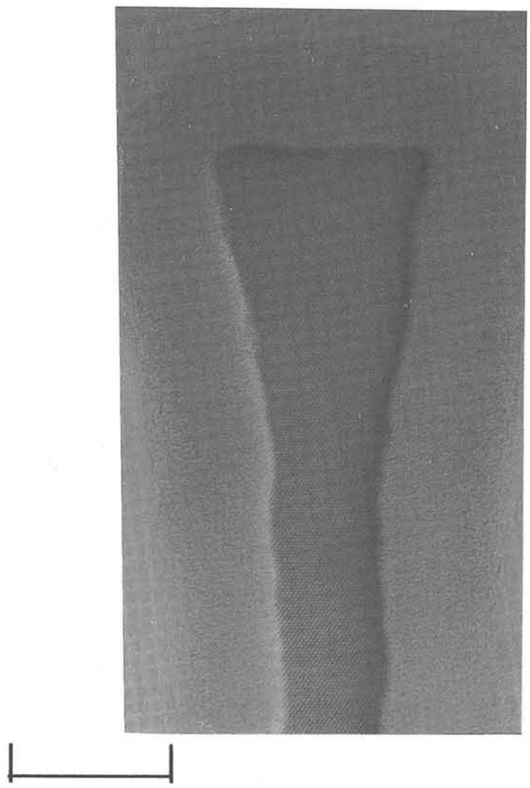


20nm

Fig.5 TEM micrograph of the Si column implanted by As($4x10^{15}cm^{-2}$, 50keV) and annealed at 1000℃. A dislocation is formed along to the {111} plane.



10nm

Fig.6 TEM lattice image of the 8nm Si column implanted by As($4x10^{15}cm^{-2}$, 50keV) and annealed at 1000℃. There is no damage in the ultra fine Si column.