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A Post Gigabit Generation Flash Memory Shallow Trench Isolation Scheme. The LATI-STI Process (LArge Tilt Implanted Sloped Trench Isolation) Using 100% CMP Planarization.

S. DELEONIBUS, M. HEITZMANN, Y. GOBIL, F.MARTIN, O. DEMOLLIENS and J.-C. GUIBERT
LETI(CEA) Dept de Microélectronique CENG 17 Avenue des Martyrs 38054 Grenoble Cedex 9 France

The optimization of a LArge Tilt Implanted Sloped shallow Trench Isolation (LATI-STI) process for Gigabit density Flash Memories is presented. The process uses 70° sloped and large tilt angle(up to 55°) implanted trench sidewalls, combined with a single step Chemical-Mechanical Polishing(CMP) planarization. A new method of NMOS subthreshold conduction analysis under strong VB conditions is demonstrated. High quality 7 nm gate oxide and 15V holding isolation are demonstrated for 0.45µm finished spacings between diffusions. The 70° sloped LATI-STI scheme allows larger process margins than the 90° sloped trenches process as far as sidewall inversion and stress induced junction leakage is concerned.

1. LATI-STI PROCESS FLOW

The planarization process and the sidewall transistor subthreshold behaviour are the main problems to solve to integrate shallow trench isolation[1),2)]. With the LATI-STI process we implemented a low cost high performance shallow trench isolation scheme for 1 Gbit density Non Volatile Memories. The process flow is shown in figure 1: 70° sloped 500 nm deep trenches are achieved after a nitride/pad oxide masking. Boron field implant can be achieved through a high temperature sidewall oxide with a large tilt angle t . Rotation is used to avoid shadowing. After trench filling, with a DCS based chemistry oxide deposition and densification, the single step CMP planarization process is applied before mask removal and further integration processing[3)].

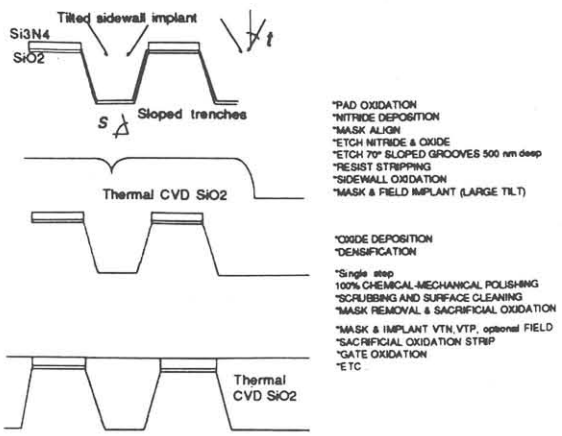


Figure 1 LATI-STI process flow

2.MORPHOLOGICAL RESULTS

Figure 2a shows a 0.70µm pitch array after polishing and HF dip. The LATI-STI process allows a void free 0.35µm finished spacings because of appropriate densification and trench slope combined with long range planarization (figure 2b). Hereafter, we have compared this process with s=80° or 90° sloped trenches and through-field-oxide retrograde 220 keV Boron implant (RETRO).

(2a)

(2b)

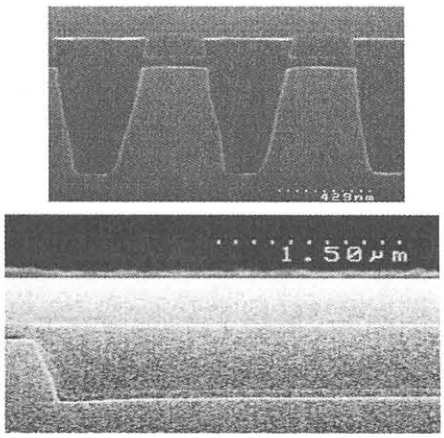


Figure 2 LATI-STI process cross section after CMP planarization : (a) 0.70µm pitch array (b) Large width trench

3.GATE OXIDE QUALITY

The 7 nm tunnel oxide breakdown field cumulative failures measured on 12 m active perimeter MOS capacitors is shown in figure 3 : less than $8x10^{-3}$ def/m is obtained for 10MV/cm breakdown field Intrinsic breakdown field is 15MV/cm. Qbd10% values higher than 1 C/cm^2 Qbd are demonstrated .

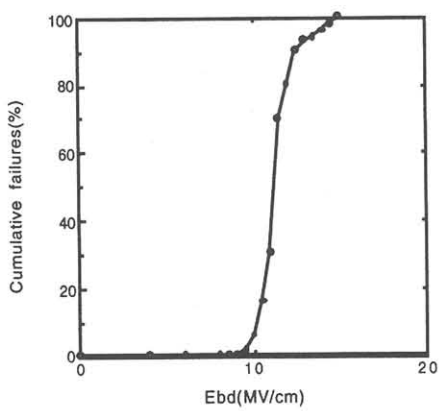


Figure 3 LATI-STI process. Cumulative failure of 7nm tunnel oxide breakdown field. 12 m active edge 420 capacitors.

4. NARROW CHANNEL AND MULTIEDGED N CHANNEL DEVICES

No narrow channel VT roll-on (narrow channel effect) is observed whatever the VB value even for implanted sidewalls: figure 4 shows the Id(Vgs) characteristics of narrow channel width devices. The multiedged gate NMOS devices characteristics(10 fingers gate L=0.8µm; W=5µm) are very sensitive to subthreshold sidewall conduction(figure 5). The subthreshold hump can be suppressed for VB=0V by using tilt implanted sidewalls In the RETRO case, the s=70° characteristics is improved as compared to the s=90° case. The VB=-10V characteristics subthreshold hump will be suppressed if LATI-STI is used with s=70° and t=55°. We consider the Vg values for a given leakage current in the strong inversion (VgS) and weak inversion(Vgw) regimes(figure 4).

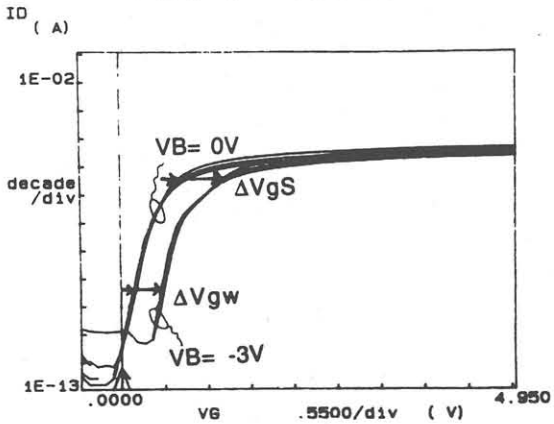


Figure 4 LATI-STI process. Subthreshold characteristics of L=0.8µm W=1; 0.6 and 0.3µm NMOS transistors at Vds=0.1V for VB=0V and VB=-3V. Tilted implant t=20°

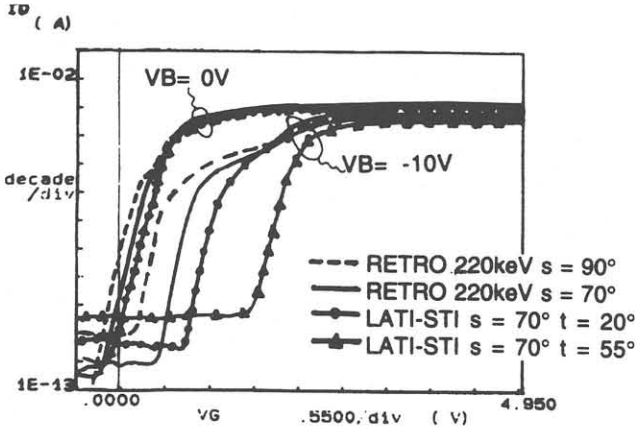


Figure 5 Subthreshold characteristics of L=0.8µm multiedged NMOS transistors(10 fingers gate) at Vds=0.1V for VB=0V and VB=-10V. Comparison of LATI-STI with retrograde implant .

5. PROCESS DEPENDANCE OF ΔVg.

The difference between Vg values at a given VB and VB=0V (ΔVg) are reported in figures 6 and 7. Compared to the case s=90°, the ΔVgw values are closer to the ΔVgS values if s=70° whatever the field implant scenario.

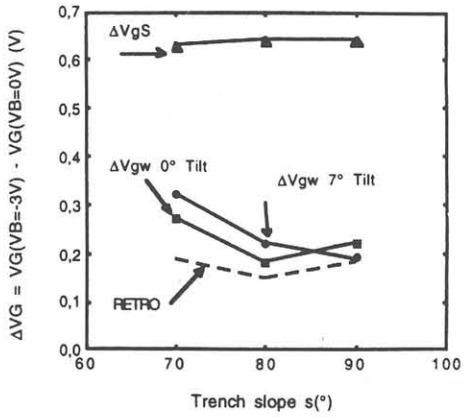


Figure 6 ΔVg as a function of trench slope. LATI-STI process. Comparison with retrograde implant(RETRO)

For large t values (t=55°), ΔVgw will reach ΔVgs because of dose loss minimization on a 70° sloped sidewall (figure 7).

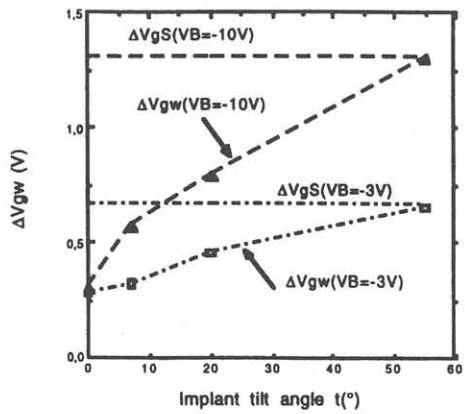


Figure 7 ΔVgw as a function of tilt angle t for VB= -3V and VB= -10V.LATI-STI process. s=70°

The sidewall implant is the best trade-off between performance and efficient sidewall doping: a dose loss minimization together with a 25% lower junction capacitance (Table 1) can be obtained with t =55 ° on a s=70° sloped sidewall.

Table 1 ΔVgw and junction capacitance values for different process conditions.

s(°)	t(°)	ΔVgw(VB=-10V) (V)	n+p (perimeter junction capacitance in pF)
70	7	0.57	115
70	55	1.30	115
70	RETRO	0.55	145
90	RETRO	0.35	140

The poly gate overhang on the active areas sidewall will impact the ΔVgw values as already reported for subthreshold slope[4]. The control of the outside corner inversion of a 70° sloped trench will be less sensitive than a 90° sloped trench to thickness variations. The ΔVgw values variations will be larger in the case of a 90° sloped

trench compared to a 70° case (figure 8). The process margins are thus larger in the 70° case.

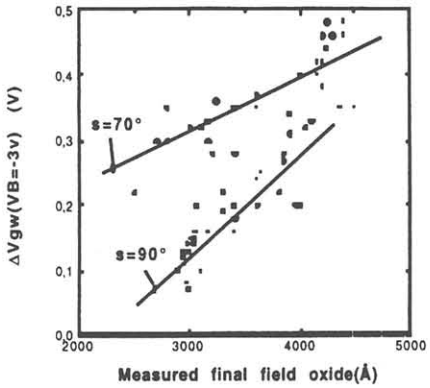


Figure 8 ΔVgw for Vb=-3V as a function of final field oxide thickness adjusted by voluntarily removed field oxide before gate oxidation. Case of tilted sidewall implant t=7°.

6. LATI-STI FIELD ISOLATION

Punch-through of n+/n+ field devices is improved by using s=70° instead of s=90° because of higher sidewall doping efficiency(figure 9): the larger the trench slope, the larger the avalanche breakdown voltage but the higher the leakage current at low Vd. 15 V punch-through voltage 0.45 µm n+/n+ finished distance is achievable with s=70° together and t=55°(figure 9).

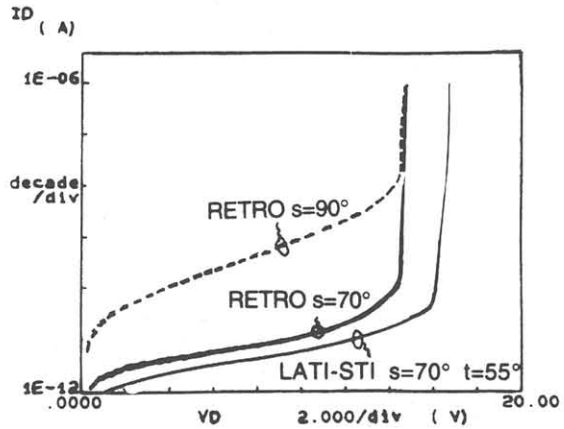
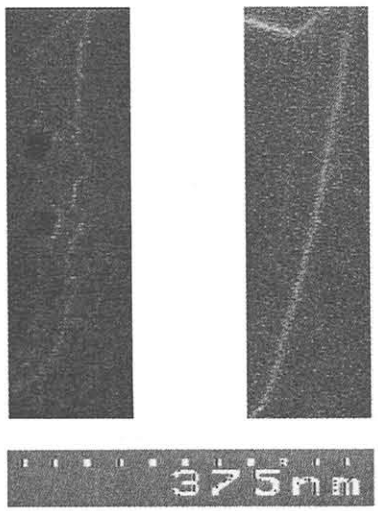


Figure 9 N+/N+ field devices punch-through I(V) characteristics N+/N+ distance is 0.45µm. Active area perimeter 2000µm. Comparison of RETRO and LATI-STI.

The differential stress induced at the refill oxide to sidewall thermal oxide interface during further processing will be larger in the case of a 90° slope compared to the 70° slope. Stress induced voiding could result in chlorine out gasing and trench sidewall pitting in the 90° case; no such defect could be observed in 70° sloped trench(figure 10). Junction leakage could then be favourized in the 90° slope case and explain the results of figure 9.



(a) (b)

Figure 10 Sidewall cross section of (a) 90° (b) 70° sloped trenches. MOS transistor sidewall. Silicon stress induced pitting is visible in the 90° case. No pitting in the 70° case. DCS, N2O chemistry refill oxide.

7. REFERENCES

1) Fuse et al. IEDM Tech. Digest, pp. 732-735, 1987
2) Davari et al. IEDM Tech. Digest, pp. 61-64, 1989
3) Deleonibus et al. Spring ECS Meeting, pp.267-268, May 1994
4) Ohe et al. IEEE Electron Devices Letters vol.13, n°12, pp636-638,1992.