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Highly Manufacturable Shallow Trench Isolation for Giga Bit DRAM

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A simple and highly manufacturable Shallow Trench Isolation (STI) process is developed for 1Gb DRAM and beyond. The main features of this STI scheme consist of dual slope trench formation and selective dry etching assisted CMP planarization. The dual slope trench is formed by utilizing polymer generation during trench etching to improve the subthreshold conduction characteristics as well as to reduce threshold voltage variation. The key ideas of dry etching assisted planarization are to form local oxide mesas by using a high selectivity dry etching, and to minimize amount of CMP(Chemical Mechanical Polishing) by simply removing the locally formed oxide mesa. As a result, this new STI process significantly reduces the dishing in the large field area and enhances the flatness between the high and sparse density areas such as cell array and periphery region in a high density DRAM. Also this STI provides hump-free transistor characteristics.

1. Introduction

In recent years, dedicated efforts have been made in order to achieve a narrow and leakage free isolation technique. So far, STI combined with CMP is regarded as one of the promising candidates for the ULSI device isolation such as high density DRAM [1,2]. However, number of problems are remained to be solved such as sub-threshold hump, dishing in large field area, and non-planarity (non uniform field oxide thickness) across a wafer. Among them, it is known that sub-threshold hump and the variation of threshold voltage are closely related to the planarity between field oxide and active Si surface (amount of field oxide recess) and the trench edge shape[3]. In this paper, a simple and stable STI process using dual slope trench and dry etching assisted planarization is introduced to overcome these problems. The process sequence is described and the results are presented. The electrical characteristics of isolation and transistor are discussed with measured data. It is concluded that this new isolation technique is suitable for 1Gb DRAM and even beyond.

2. Fabrication procedure

In this section, the process sequence is discussed. Fig.1 shows the STI fabrication procedure. Active regions with 0.2μm design rule are defined by deep UV(KrF) lithography[Fig. 1(a)], and the 0.4μm depth of trench is formed by ME-RIE using masking layers(150nm HTO/ 200nm SiN/ 10nm Pad oxide). A trench side-wall oxidation (160nm) is followed to cure the damaged silicon and to passivate silicon surface from TEOS (700nm) oxide as a filling material. Having filled the trench [Fig.1(b)], the selective oxide etching is done by the opening patterns in periphery region and island patterns in cell array region[Fig. 1(c)]. After this selective oxide etching, only locally formed narrow width oxide spikes exist along the boundary between active and field in the periphery region. And locally formed oxide pillars remain on the field in cell array region. As a result, this step greatly reduces thickness of the deposited oxide on active regions, and minimizes the amount of oxide to be polished. Therefore, it prevents the dishing commonly happened in CMP based STI[4]. The next process is oxide CMP (~300nm) planarization [Fig. 1(d)]. After then, 0.20μm design rule CMOS is fabricated with a retrograde twin-well, 7nm gate oxide and polycide gate. Fig.2 shows the dual slope profile made from polymer generation process during trench etching in a Cl2/HBr ambient[5]. The angle of first slope is 45 degree and the length is 50nm. The angle of second main slope is 80 degree and the depth is 0.4μm. Fig.3 shows the oxide pillars built in the cell array after dry etching, and these pillars reduce dishing in the cell array.

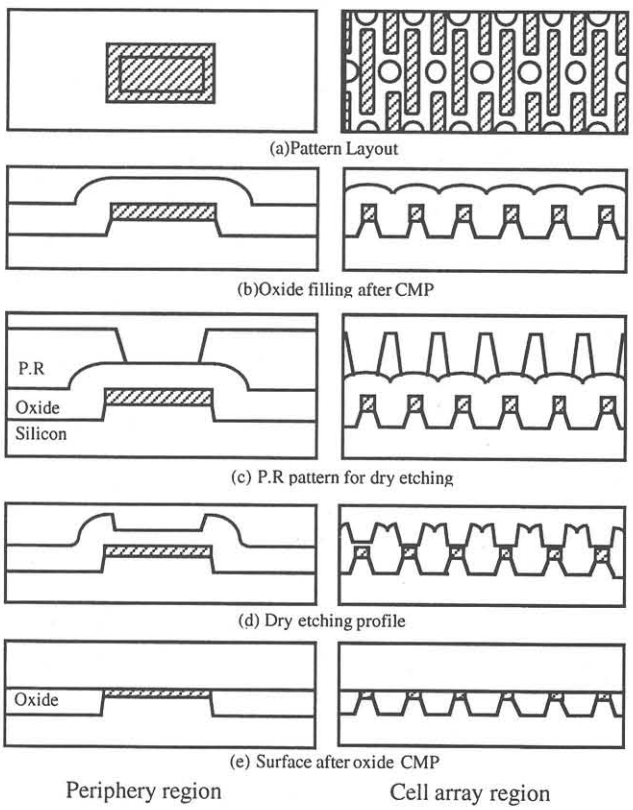


Fig. 1 Process sequence of STI

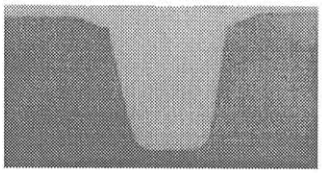


Fig. 2 Doubly tapered trench profile
Taper(45°,length=50nm), Trench(80°,depth=0.4μm)

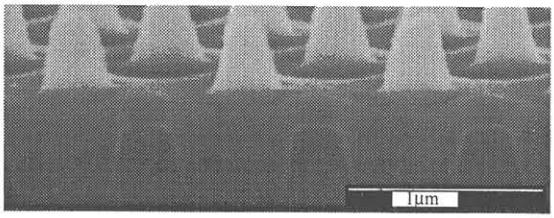
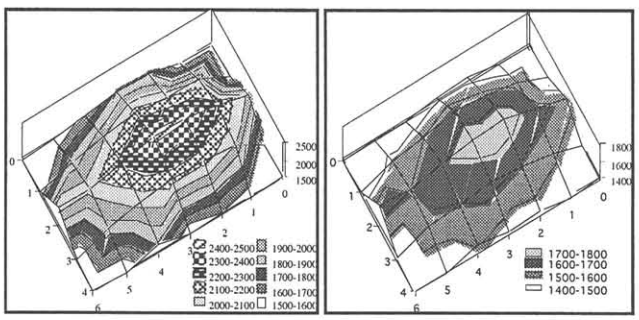


Fig. 3 Remaining oxide pillars in the cell array after dry etching

3. Results and Discussion

(1) Physical Uniformity

Fig. 4(a) shows the uniformity of the oxide thickness after oxide dry etching measured by ellipsometer(FE-IV) at 23 monitoring points across a 6-inch wafer. The remaining oxide is thickest at the center region, and thinnest at the edge region. This difference is less than 100nm, and comes from the combined result of the previous steps (trench, filling, and dry etching). Fig.4(b) shows the thickness of mask layer(SiN) reduced to 40nm in difference after oxide CMP (~300nm). This is a better result compared to previous paper[6]. Fig.5 shows the center and the edge surface in periphery and cell array on the wafer after CMP, and the SiN loss less than 100nm is realized in the cell array. Excellent planarization in all of the regions is achieved.



(a) Oxide thickness on the mask layer(SiN) after dry etching (b) Mask layerthickness(SiN) after Oxide CMP

Fig. 4 The contour of the thickness across the wafer

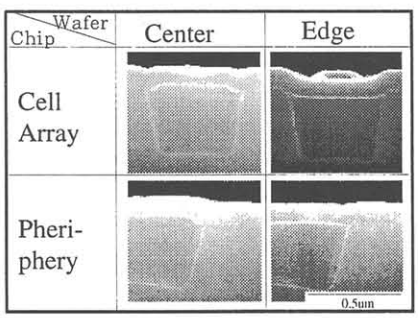
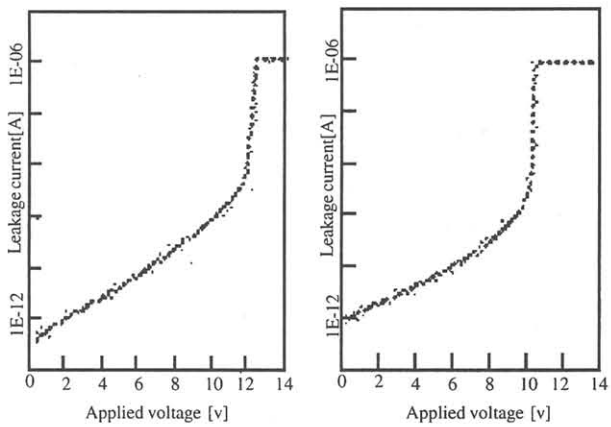


Fig. 5 Surface topography after CMP on various location of wafer

(2) Electrical Characteristics

Fig.6 shows the electrical characteristics of the shallow trench isolation (space=0.24μm). Both of N+ and P+ isolation have leakage current less than 5fA/μm at 5V. And the break-down voltages of these isolations are greater than 12V. These values are sufficient enough for ULSI devices such as 1 Gb DRAM. Fig.7 shows sub-threshold characteristics of the cell transistor of size, W/L=0.2μm/0.2μm. No sub-threshold hump is observed. The distributions of threshold voltage and sub-threshold swing are shown in Fig.8. NMOS devices with gate length 0.30μm have threshold values from 0.556V to 0.610V. The difference across the wafer is less than 54mV. PMOS devices with gate length 0.40μm have threshold values from 0.532V to 0.620V. The difference across the wafer is less than 70mV. The variation of the sub-threshold swing is less 5% for NMOS, and 10% for PMOS. The above values of threshold voltage and sub-threshold swing are sufficient for 1Gb DRAM circuit operation. No measurement shows sub-threshold hump owing to the optimized trench profile and the excellent planarity of surface(no field oxide recess) across the wafer.



(a) N+ to N+ Isolation (b) P+ to P+ Isolation

Fig. 6 Isolation characteristics of N+ to N+ and P+ to P+ ,space=0.24μm,width=30000μm

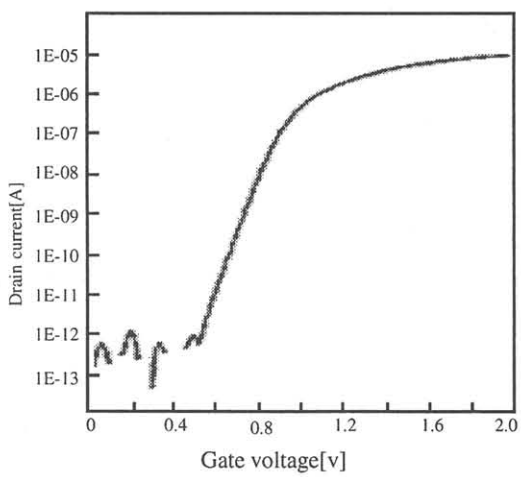
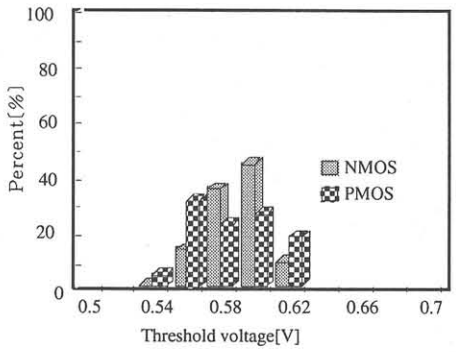
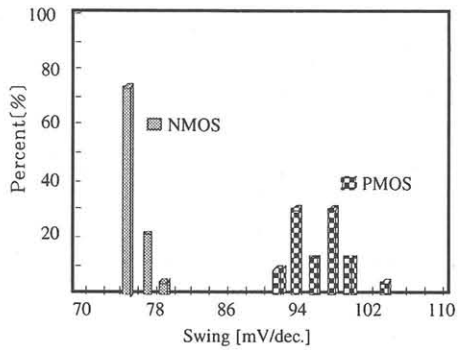


Fig. 7 Sub-thresholdchracteriscics of 0.2μm/0.2μm cell transistor,Tox=7nm



(a) Distribution of the threshold voltage



(b) Distribution of the sub-threshold swing

Fig. 8 Distribution of the electrical parameters; threshold voltage and Sub-threshold swing

Fig. 9 shows a narrow width effect of the transistors with STI. Both of NMOS and PMOS do not show threshold voltage roll-off down to active width 0.2μm. The interface state of the tapered trench edge is electrically estimated by the field transistor. Fig.10 shows its breakdown voltage (@10nA, width=100μm) having constant values with respect to the isolation size.

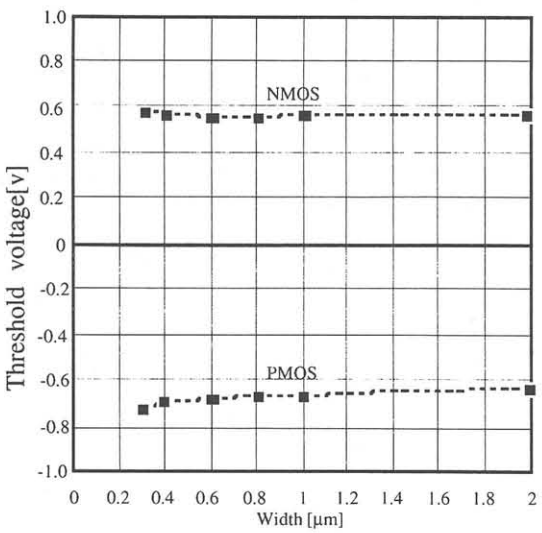


Fig. 9 Narrow width effect of the transistor ;Length=0.34μm(NMOS),0.44μm(PMOS)

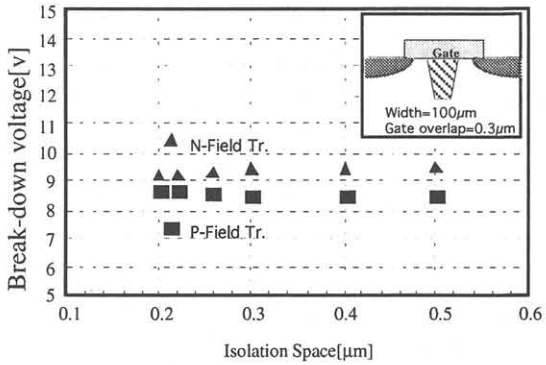


Fig. 10 Break-down voltage of the field tansistor with spaces

4. Conclusion

A highly manufacturable STI process is developed for 1Gb DRAM by using dual slope trench profile and dry etching assisted CMP planarization. This STI provides good electrical characteristics and excellent physical planarity across the wafer.

5. References

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