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Large Diameter Epitaxial Wafers for Future ULSI

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The use of epitaxial silicon wafers for state of the art silicon wafers for state-of -the-art integrated circuits continues to get increased attention. Past emphasis in production use has been on latch-up control in logic designs. However, as device processing moves toward 0.18-0.25μ design rules and wafer diameters move toward 300 mm, several forces are at work to predict a much broader use of epi for ULSI devices in the next one to two technological generations. The necessity of finer defect control and the trends in relative costs between polished and epi wafers tend to support the potential choice of epi material.

1. INTRODUCTION

Epitaxial wafers may well enjoy a much broader usage in IC processing in the near future. Though many exciting technological steps may occur, it still remains that the movement will be supported by arguments that are based in favorable economics for large scale mass production.

2. DESIGN CONSIDERATIONS

The use of epitaxial wafers for integrated circuits offers several possible advantages. Epi first was recognized as providing improved storage time (refresh) characteristics in dynamic RAMs made with NMOS processing[1]. Figure 1 shows an example of such improved performance, particularly as the operating temperature increases[2]. However, these results did not justify the added cost of using epi, and essentially all NMOS dRAM processes in the past remained on(or returned to) polished wafer substrates.

Today the majority of ICs involve some form of CMOS processing. Recognized positive epi effects include:

a. Latch-up Control. Latch-up phenomena relate to parasitic transistors being formed between the source/drain regions and the tubs in CMOS processing[3]. Large sustained currents are produced that make the device fail. This phenomena can be reliably controlled by using an epi layer on a heavily doped substrate to significantly reduce the resistance this current sees. Careful design scaling can avoid this issue,

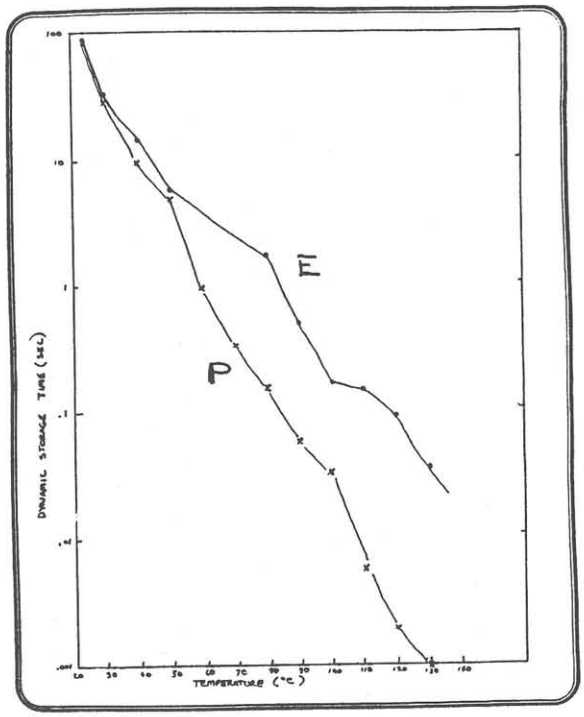

Fig. 1. Dynamic storage time for 64k dRAM-Epi vs. PW[2]

and that is feasible under certain conditions on devices such as dRAMs. However, when complex circuits such as microprocessors are considered, scaling issues are much more difficult and epi is widely used.

b. Trench capacitor design. The use of epi wafers with heavily doped substrates for trench capacitor designs is an enabling technology to allow such a device to work. A typical cell is shown in Fig. 2[3]. This type of device allows a thinner depletion layer and can help with soft errors due to radiation.

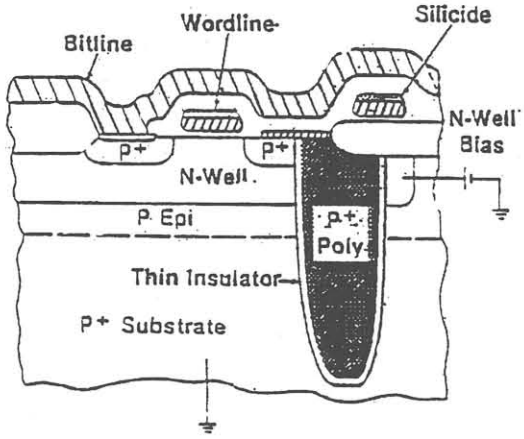

Fig. 2. Trench capacitor cell structure[3]

c. Defect control. As device designs are shrunk there is a sensitivity to smaller and smaller defects. Silicon crystals have been shown to have various defects in the near surface of 0.1μm or less. An epi layer can provide a more completely defect free region on which to build devices. This can be a part of several benefits from an epi wafer utilizing a heavily doped substrate, or it can actually be with an epi layer on a wafer doped at the same levels as the epi for the purpose of defect control alone[4,5]. Fig. 3 shows results for dRAMs where the number of failed individual bits is improved by using epi on a lightly doped wafer.

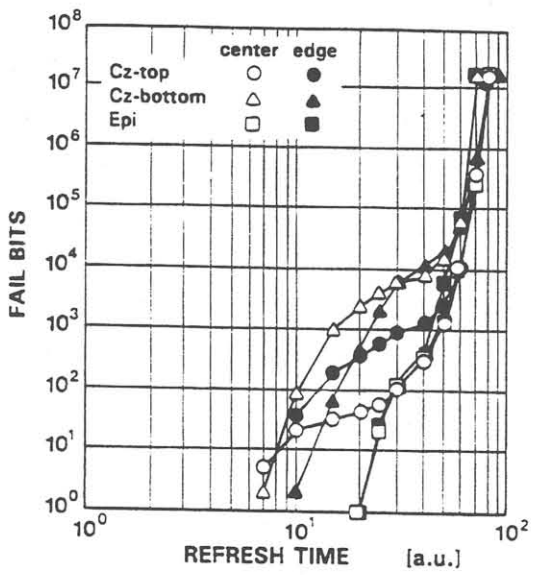

Fig. 3. Pause tail characteristics on dRAM devices[4]

3. LARGE DIAMETER EPI SPECS

As a move to 300 mm wafers appears realistic in the near term, it is important to recognize the areas where specifications are critical for success. It is not possible to totally separate the changes that relate specifically to the diameter itself and those that occur because of the current design requirements. However, the following comments can be made:

a. Wafer backside finish. It is anticipated that 300 mm wafers will generally be double side polished. This will reduce the sensitivity to particle generation and may contribute to wafer strengthening.

b. Edge finish. The edge of 300 mm wafers will be polished. This will generally contribute a toughening of the wafer, as well as particle reduction. This may be necessary to control slip in thermal processing, particularly the epi process itself.

c. Epi backseal. Oxide layers used on epi wafers to control autodoping will be avoided, or at least made much thinner. The effect of the stress from this layer as well as those in the device processing will require much study and careful control for 300 mm wafers.

d. Epi substrate resistivity. Epi substrate resistivity is projected to be P-type and very heavily doped (nominally 0.008 ohm-cm). This will add strength to the wafer as well as design flexibility. However, other problems are increased, such as with autodoping and transition widths.

e. Epi layer thickness. The thickness of the epi layer will continue to be thinner, in the range of 1- 3 μm. Thickness tolerances, while not particularly critical for latch-up must be tightened for optimum trench capacitor design.

f. Light point defects. The control of particles and other LPD of a diameter of 0.1 μm or less is crucial to make good devices. As noted earlier, the use of epi eliminates certain classes of defects.

g. Other. Specifications of other parameters such as site flatness or metallic contamination will, of course, continue to get a lot of attention

for new processes; but that will be true whether or not the wafer has an epi layer and whether or not it is manufactured at 300 mm diameter.

4. EPI REACTORS FOR 300 MM

The design of epi reactors for large diameters moved batch to single wafer processing for 200 mm wafers. This technology allows the use of high growth rates and a rotating susceptor to provide a wafer with much improved layer resistivity and thickness uniformities with good productivity[6]. A typical single wafer chamber is shown in Fig. 4. This type of process can be in stand-alone units or clustered. The first generation of epi for 300 mm is expected to be a scale-up of this same technology, and there is some expectation that overall unit (area) productivity can be improved on 300 mm.

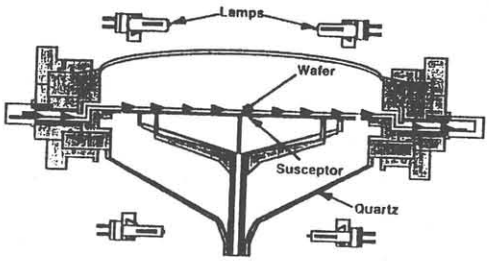

Fig. 4. Single wafer chamber for epi deposition[7]

5. ECONOMIC CONSIDERATIONS

When the choice is made as to whether or not to use epi on a particular device process, the analysis is quickly reduced to a comparison of the relative cost of epi wafers and polished wafers. The cost difference is then is compared to the yield or parametric advantages obtained by using epi. This includes analyzing the advantages to employing certain device technologies that are impossible without epi. Figure 5 shows the trend of relative costs for epi and polished wafers as a function of diameter. For 300 mm, it is expected that the E/P ratio will continue to reduce, to possibly 1.5 X or less. This trend occurs, of course, by a combination of improving epi processes, and certain costs that are increased in the polished wafer itself. As was already mentioned, the extension of current single wafer epi technology to 300 mm offers possible cost improvements. On the other hand, the costs involved in extending silicon crystal growth to 300 mm will probably increase more than the proportional area increase.

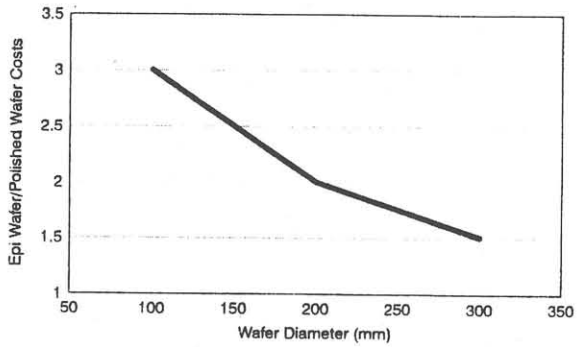

Fig. 5. E/P Cost ratio by diameter

6. CONCLUSION

The two most critical issues influencing the use of epi for MOS processes in the future are the relatively favorable trend of the cost of epi versus polished wafers and the incredibly tight requirements that will exist for defect control. This combination clearly points to epi as a favorable choice, and in certain circumstances may make epi the only choice.

References

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