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Deep Levels and Conduction Mechanism in Low-Temperature GaAs Grown by Molecular Beam Epitaxy

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Deep levels in low-temperature (LT) GaAs layer grown by molecular beam epitaxy were investigated by deep level transient spectroscopy (DLTS), photocapacitance and photoluminescence (PL) techniques. For the LT-GaAs layers grown at 350°C, five electron traps were detected, and the trap concentration of the dominant deep level (S1) was found to be $1.8 \times 10^{16} cm^{-3}$ with an activation energy of 0.64eV. The S1 level showed remarkable photoquenching behavior. The electrical conduction in LT-GaAs seems to be governed by these traps with high density.

1. INTRODUCTION

Recently, GaAs layers grown at low temperatures by molecular beam epitaxy (the so-called LT-GaAs) have attracted considerable attention due to their useful properties for device applications such as reduced side-gating in GaAs MESFETs and HEMTs, removal of surface Fermi level pinning, ultra-fast optical switching and optical non-linearity. However, the electrical conduction mechanism of LT-GaAs layers have not been clarified yet, being disputed between a model based on cluster of EL2-like levels[1] and a model based on As cluster-induced Fermi level pinning[2].

The purpose of this paper is to try to detect deep levels and clarify the electrical conduction mechanism in the LT-GaAs layers by using current-voltage (I-V), deep level transient spectroscopy (DLTS), photocapacitance and photoluminescence (PL) techniques.

Deep levels in LT-GaAs have been studied by many different experimental techniques. However, the DLTS technique, one of the most common methods of defect studies, has rarely been applied, because of the semi-insulating properties of LT-layers. In this investigation, we have prepared conductive LT samples by Si doping so as to apply the DLTS technique.

2. EXPERIMENTAL

The LT-GaAs layer was grown by standard MBE system on n^+-GaAs (100) substrates. Prior to growth, the substrates was thermally cleaned to remove native oxide, and then cooled down to the growth temperature T_g. T_g was changed within a range of 250-400°C, was monitored by combined use of a thermocouple and a pyrometer. The thickness of the LT-GaAs layer was typically 1μm, and the growth rate was 8000Å/h. After the growth, all the samples were annealed at 580°C for 5 minutes in the MBE chamber with an As_4 overpressure.

The cross-sections of the samples used on this study are schematically shown in Fig. 1. Two types of sample structures were used in this study. Type (a) sample contains undoped LT-GaAs layer grown at 250°C and was used for I-V and PL measurements. (In the case of PL measurement, a semi-insulating substrate was used.) And type (b) sample contains a Si-doped LT-GaAs layer grown at 250°C- 580°C and was used for C-V, DLTS and photo-capacitance measurements.

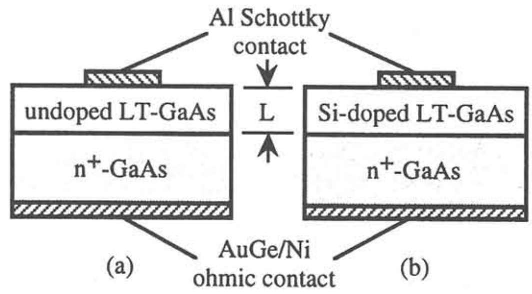


Fig. 1 Sample structures.

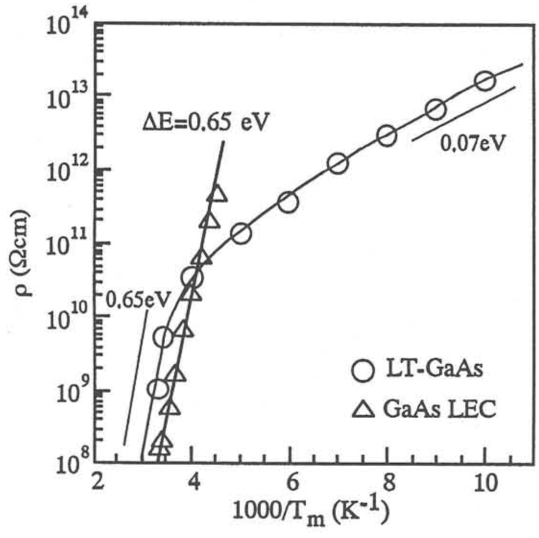
3. RESULTS and DISCUSSION

3.1 *Electrical Conduction Characteristics*

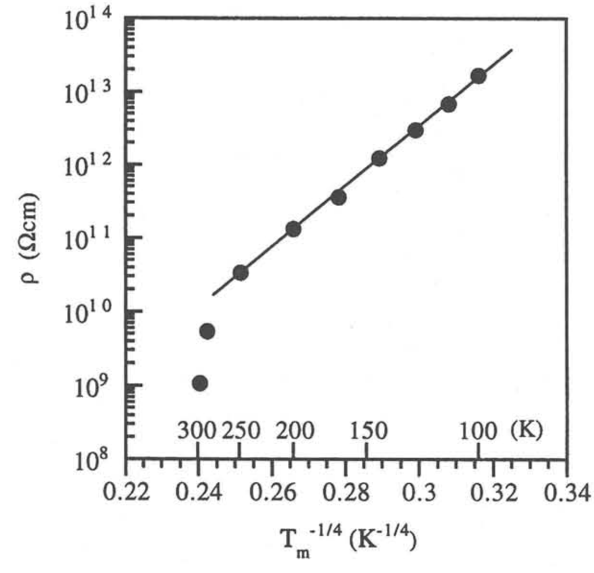
In Fig. 2(a), the arrhenius plots of resistivity (ρ) of the undoped sample are shown vs. the reciprocal of the measurement temperature (T_m). For comparison, the data on a semi-insulating liquid-encapsulated Czochralski (LEC) GaAs substrate is also shown. As seen in Fig. 2(a), conduction in the LT-GaAs layer cannot be described by a single thermal activation energy as in the LEC material. Such behavior was also reported by other groups [1, 3]. On the other hand, the ρ vs. $T_m^{-1/4}$ plot gave a straight line above 250K, as shown in Fig. 2(b), giving a picture that presence of a high density of deep traps with the activation energy of 0.65eV gives rise to a variable-range hopping at low temperature (<250K), while band conduction becomes dominant over hopping at higher temperatures (>250K).

3.2 *Deep Levels in LT-GaAs*

Figure 3 shows Schottky C-V characteristics of the Si-doped ($5 \times 10^{16} cm^{-3}$) samples grown at various low-temperatures. For the growth temperatures of T_g=350°C and 400°C, the layers showed n-type conduction, whereas the layers become semi-insulating for T_g=300°C and 250°C.



(a)



(b)

Fig. 2 Temperature dependence of resistivity.

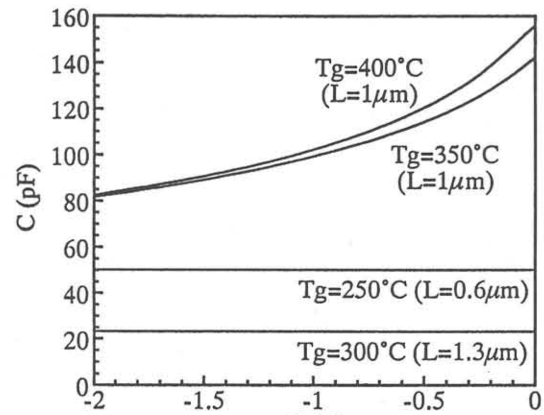


Fig. 3 Schottky C-V curves.

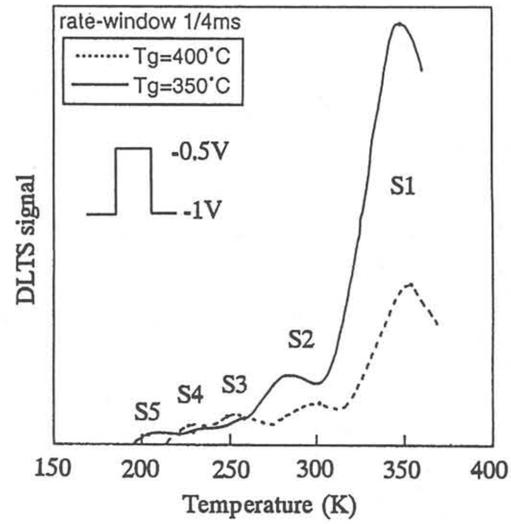


Fig. 4 DLTS spectra of LT-GaAs.

Based on the results of C-V characterization, DLTS spectra of Si-doped conductive LT-GaAs layers were measured. For samples grown at 580°C, no significant DLTS peak was detected within the detection limit of $1x10^{13}cn^{-3}$. DLTS spectra obtained for the samples grown at 350°C and 400°C are shown in Fig. 4. Five traps (labeled S1-S5) were detected in the grown layers. The concentration of the dominant trap (S1) was determined to be $8.1x10^{15}cm^{-3}$ for T_g=400°C and $1.8x10^{16}cm^{-3}$ for T_g=350°C, respectively, taking into account the so-called λ effect,[4] i.e., the effect of the width of the region of the unionized deep levels in the depletion region.

In Fig. 5, the arrhenius plots for the observed five electron traps are compared with those of the known traps in normal bulk and epitaxial GaAs and with those of traps detected in LT-GaAs by Martin et al.[5] (EL2-EL6), Lang et al.[6] (EB3-EB7), Puechner et al.[7] (P1-P3) and Lin et al.[8] (EAL1-EAL3). The activation energies for the traps, S1-S5, are 0.64eV, 0.56eV, 0.46eV, 0.38eV and 0.33eV, respectively. The plot of S1 is similar to that for EB4 which is produced by irradiating GaAs epitaxial layer by electron beam and believed to be related to As_{Ga}-defect complexes[9, 10].

The growth temperature (T_g) dependence of the trap concentration (N_t) of the dominant level (S1) is plotted in Fig. 6. The data of LT-GaAs layer grown at 200°C reported by Look et al.[11] (IR absorption) is also included. They also detected EB4-like levels in LT-GaAs grown at 400°C and 450°C by DLTS[12], and suggest that the levels were dominant compensation centers. The result of Fig. 6 indicates that the concentration of S1 level drastically increases with decreasing the growth temperature.

In order to investigate the nature of the S1 trap in more detail, photocapacitance and PL measurements were performed. Figure 7 shows typical photocapacitance transient of the layer grown at 350°C. As shown,

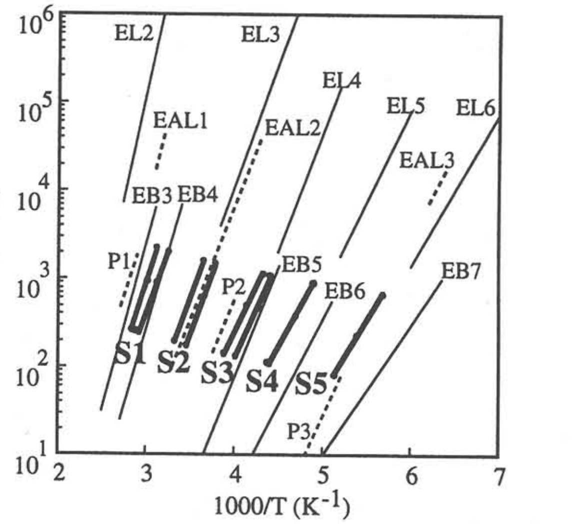


Fig. 5 Arrhenius plots of deep levels (S1-S5) observed in LT-GaAs.

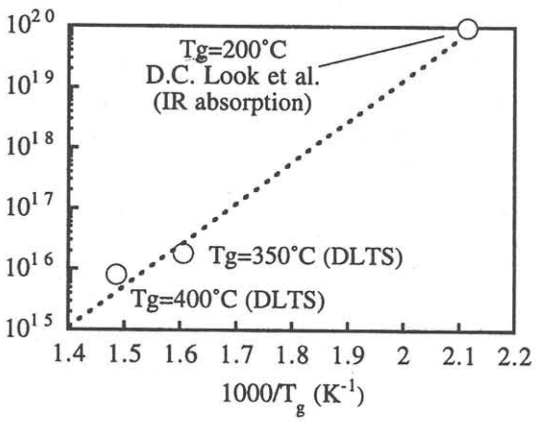


Fig. 6 Growth temperature dependence of trap concentration.

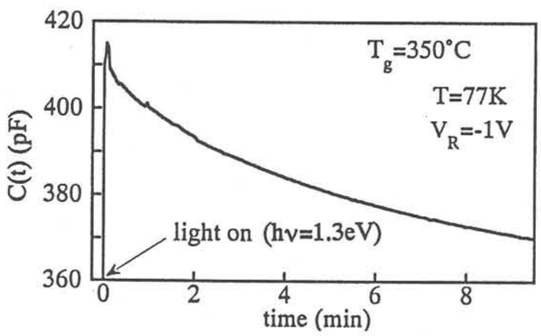


Fig. 7 Photocapacitance transient under illumination.

capacitance of the Si-doped LT-GaAs layer was found to exhibit photoquenching under illumination (hν=1.3eV) at 77K. The trap density estimated from the quenched capacitance is about $2x10^{16}cm^{-3}$, and is in agreement with the density of S1 trap obtained by DLTS measurement. This indicates that the dominant deep trap, S1, in LT-GaAs layer has a similar property with EL2.

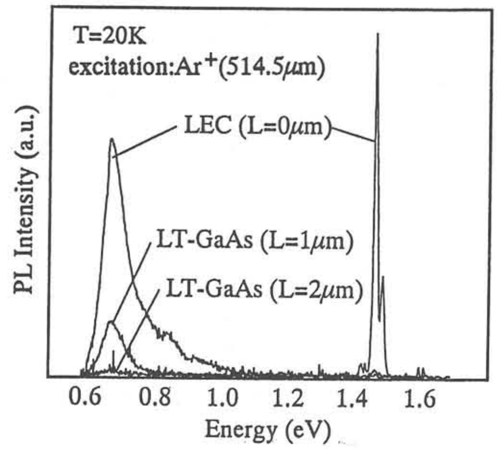


Fig. 8 Photoluminescence spectra of LT-GaAs layers.

The result of PL measurement from LT layers grown on LEC semi-insulating substrates is shown in Fig. 8. No appreciable PL signal is observed, and peaks at 0.68eV and 0.8eV commonly observed in EL2 containing materials are hardly observed. From these results, the dominant trap in LT-GaAs seems to be one of the EL2 family since the S1 trap exhibited a clear photoquenching phenomenon. However, difference in the signature plot as well as absence of PL indicates that it is not EL2 but a new EL2-like center having a different defect micro-structure.

4. CONCLUSION

The electrical conduction behavior and deep level properties in LT-GaAs were studied. The conduction in LT-GaAs layers seems to be governed by high density of S1 trap with the activation energy of 0.64eV. Similarly to EL2, S1 trap shows photo-quenching effect but its signature plot and PL property are very different. It appears very difficult to explain the present results by the model based on Fermi level pinning by As clusters.

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