Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 392-394

Lateral Tunneling Devices on GaAs (111)A and (311)A Patterned Substrates Grown by MBE Using Only Silicon Dopant

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A lateral interband tunneling transistor with gate-controlled negative differential resistance characteristics is demonstrated for the first time on a GaAs(111)A patterned substrate. Si-doped GaAs layers are grown on GaAs(111)A and GaAs(311)A patterned substrates by molecular beam epitaxy to fabricate lateral p-n junctions. Both samples show interband tunneling diode characteristics. Furthermore, a gate electrode is fabricated on the (111)A sample. The lateral tunneling transistor shows the modulated peak current density from 0.41 to 0.90 mA/cm^2 by varying the gate voltage from -5.0 to 5.0 V.

1. Introduction

Tunneling devices with negative differential resistance (NDR) characteristics have attracted much interest because of their great potential for high-speed, low-power, and multifunctional device applications due to their unique current-voltage (I-V) characteristics. Tunneling diodes[1,2] are already being used for high-frequency generation, frequency conversion and switching applications. Recently some reports have been made for three-terminal tunneling devices, that is tunneling transistors, with gate-controlled NDR characteristics[3-6] because tunneling transistors have a number of potential applications. However, there are still some problems with the device fabrication processes; they require a complicated process to fabricate the gate electrode onto vertical tunneling junctions[3-5] or require a regrowth process to obtain lateral tunneling junctions.[6]

In this paper, we propose a new fabrication technology and device structure of a tunneling transistor based on lateral interband tunneling. To achieve lateral p-n tunneling junctions, plane-dependent Si doping in nonplanar epitaxy is used.[7,8] This technique utilizes the amphoteric nature of Si dopant in molecular beam epitaxy (MBE). Since Si atoms incorporate as an acceptor in GaAs growth on (N11)A (N≤3) substrates,[9] a lateral p-n junction can be obtained by growing a Si-doped GaAs layer on a patterned (N11)A substrate. The fabrication process of the proposed tunneling transistor is as simple as that of conventional metal-insulator-semiconductor field effect transistors.

2. Experimental procedure

Patterned semi-insulating (111)A and (311)A oriented GaAs substrates were prepared using conventional photolithography and selective etching techniques. The sidewall orientations were controlled by varying the compositions of $HF+H_2O_2+H_2O$ mixtures used as etching solution.[10] A (511)A surface and (100) surface were used as the sidewall orientation for the (111)A substrate and (311)A substrate, respectively. After removing the photoresist, the substrates were degreased and etched with $NH_4OH:H_2O_2:H_2O$ (2:1:96) for 1 min at 20°C.[11] Then, they were introduced into the MBE chamber. After thermal cleaning at 630°C under an As_4 pressure, a undoped GaAs buffer layer and Si-doped (Si: $5x10^{19}$ cm^{-3}) GaAs layer were grown sequentially at 540°C. The As_4/Ga flux ratio was 5 for the (111)A substrate and was changed to 2 for the (311)A substrate to obtain a p-type layer, because the conductivity type of Si-doped GaAs layers depends on the growth conditions such as the flux ratio.[12] The growth rate was 0.6 μm/hour and the substrates were rotated at 36 rpm to expose the entire flat surface and sidewall to the molecular beam during the growth of one monolayer.

Photolithography and lift-off techniques were employed to fabricate a lateral transistor as proposed in Fig. 1. First, mesas were etched with $H_3PO_4:H_2O_2:H_2O$ (3:1:50) solution to isolate the diodes. The p-type ohmic electrode (Mn/Au) and the n-type ohmic electrode (AuGe/Ni/Au) were evaporated on the flat surface and on the sidewall, respectively, and they were alloyed at 400°C for 2 min in

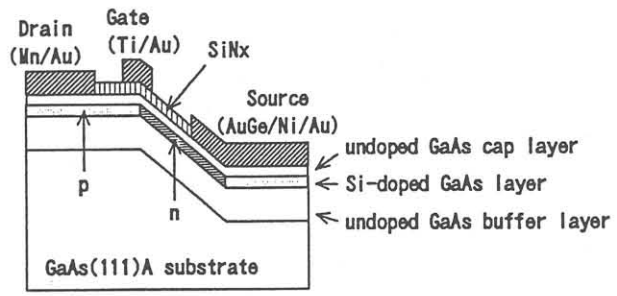

Fig. 1. Schematic cross sectional view of a lateral transistor.

N_2. Secondly, a 50 nm thick SiNx film was deposited as the gate insulator. Then, a 5 μm long and 200 μm wide gate electrode (Ti/Au) was formed by deposition on the SiNx film at the p-n junction.

Cross sections of the lateral p-n junctions were observed by scanning electron microscopy (SEM). The carrier concentrations and conductivity types of the Si-doped GaAs layers were evaluated using samples grown on planar substrates by van der Pauw Hall measurements at room temperature (RT). The I-V characteristics of the devices were measured with the HP4142B and HP16276B at temperatures from 30 K to RT.

3. Results and discussion

3.1 Lateral tunneling diodes

Figure 2 shows cross-sectional SEM micrographs of samples grown on (111)A and (311)A patterned substrates. An extra (411)A facet can be seen on the top of the sidewall for both samples. The conductivity type evaluated using Si-doped (Si: 5×10^{19} cm^{-3}) GaAs layers grown on planar (111)A and (311)A was p-type (p=5×10^{19} cm^{-3}) and that on (411)A was n-type (n=9×10^{18} cm^{-3}). These results indicate that the p-n junction is formed between the p-type top surface and the n-type (411)A facet.

I-V characteristics at RT for lateral diodes on (111)A and (311)A patterned substrates are shown in Fig. 3. NDR characteristics can be seen for both samples in the forward bias region. For the (111)A diode, the peak-to-valley ratio (PVR) and the peak current density (I_P) are 5.5 and 240 mA/cm^2, respectively. These characteristics are comparable with the (311)A diode's with a PVR of 4.0 and an I_P of 790 mA/cm^2. In the reverse bias region, the I-V characteristics of these diodes were almost independent of the measurement temperature. This result indicates that the NDR characteristics are caused by the interband tunneling phenomenon. It should be noted that NDR characteristics were not observed in a patterned (111)A substrate with a

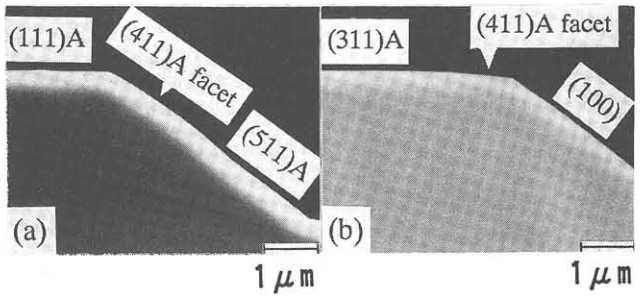

Fig. 2. Cross-sectional SEM micrographs of Si-doped GaAs layers grown on patterned substrates. (a) (111)A patterned substrate and (b) (311)A patterned substrate.

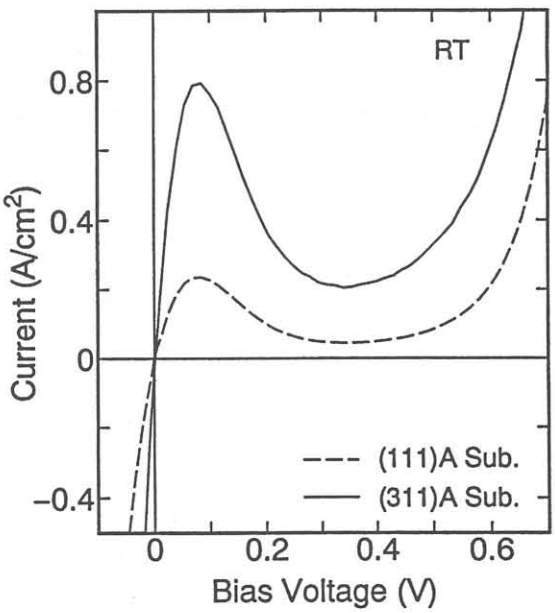

Fig. 3. I-V characteristics of lateral diodes fabricated on (111)A and (311)A patterned substrates.

(211)A or (311)A sidewall. In these samples, moreover, the (411)A facet was not observed on the top of the sidewall.[13] These results indicate that the interband tunneling phenomenon results from an abrupt p-n junction between the top surface and the (411)A facet.

To increase the peak current density, a multiple quantum well (MQW) structure was grown on the patterned (111)A substrate. This AlGaAs/GaAs MQW structure consisted of five 8 nm thick Si-doped GaAs well layers sandwiched by 30 nm thick undoped $Al_{0.2}Ga_{0.8}As$ barrier layers. In this case, the NDR characteristics were caused by the tunneling phenomenon between the p-type subband on the (111)A surface and the n-type subband on the sidewall. The peak current density was 350 mA/cm^2; this value is 1.5 times larger than that of a 0.5 μm thick GaAs lateral interband tunneling diode with the same Si doping concentration on a (111)A patterned substrate. This

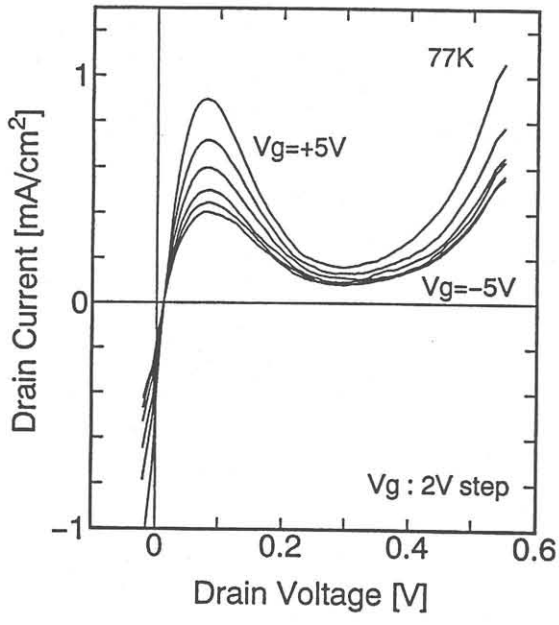

Fig. 4. I–V characteristics of a lateral transistor fabricated on a patterned GaAs(111)A substrate at 77 K.

improvement is attributed to an increase in the number of states per unit energy by vertical quantum confinement in QWs compared with a GaAs bulk structure. Furthermore, the peak current density will be increased by using MQW structures with a higher barrier height and a thinner well width.

3.2 Lateral tunneling transistors

To fabricate the lateral transistor as proposed in Fig. 1, the structure of the Si doped GaAs layer grown on the patterned (111)A substrate was as follows: a 0.6 μm undoped GaAs buffer layer, a Si-doped (Si: 1×10^{19} cm^{-3}) 50 nm thick GaAs layer and a 10 nm undoped GaAs cap layer. Figure 4 shows drain current (I_d) – voltage (V_d) characteristics at 77 K. The V_d is swept from −0.02 to 0.55 V with the gate voltage (V_g) applied in steps of 2.0 V from −5.0 to 5.0 V. The NDR characteristics are controlled by V_g. The peak drain current density is modulated from 0.41 to 0.90 mA/cm^2. On the other hand, the PVR of 5 is maintained in this gate bias region.

We have demonstrated that a lateral interband tunneling transistor can be achieved by using a Si-doped GaAs layer grown on a patterned (111)A substrate. This technique provides a simple process for fabricating three-terminal tunneling devices.

4. Conclusion

We have demonstrated lateral interband tunneling diodes by using Si-doped GaAs layers grown on GaAs (111)A and (311)A patterned substrates. The interband tunneling phenomenon is observed between the p-type layer on the (111)A or (311)A surface and the n-type layer on the (411)A facet formed on the top of the sidewall. These diodes have NDR characteristics in the forward bias region at RT. Furthermore, we have demonstrated a lateral interband tunneling transistor on the patterned GaAs(111)A substrate. This transistor has gate-controlled NDR characteristics in the forward drain bias region. The peak drain current density is modulated from 0.41 to 0.90 mA/cm^2 by varying the gate voltage from −5.0 to 5.0 V. On the other hand, the PVR of 5 is maintained in this gate bias region.

Acknowledgement

The authors would like to thank Dr. Hideyuki Inomata for his encouragement throughout this work.

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