

A Buried-Channel WN_x/W Self-Aligned GaAs MESFET with High Power-Efficiency and Low Noise-Figure for Single-Chip Front-End MMIC in Personal Handy Phone System

Kazuya NISHIHORI, Atsushi KAMEYAMA, Yoshiaki KITAURA, Yoshiko IKEDA, Masami NAGAOKA,
Yoshikazu TANABE, Masakatsu MIHARA, Misao YOSHIMURA, Mayumi HIROSE and Naotaka UCHITOMI

*ULSI Research Laboratories, Toshiba Corporation
1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan*

Microwave performance is presented for the buried-channel WN_x/W -gate self-aligned GaAs MESFET (BC-MESFET) with the combined process of ion-implantation and epitaxial growth. The $0.6\ \mu\text{m} \times 1\ \text{mm}$ FET has a power added efficiency of 57 % at 1.9 GHz and the $0.6\ \mu\text{m} \times 100\ \mu\text{m}$ FET has a minimum noise figure of below 0.4 dB at 2 GHz. These results demonstrate that the BC-MESFET is suitable for single-chip front-end MMIC in personal handy phone system.

1. INTRODUCTION

Recently, the mobile communication has advanced to the L-band personal handy phone system (PHS). The PHS includes several blocks; RF transmission, RF reception, RF switch, and so on. The integration of these blocks in a single-chip MMIC is one of the preferred approaches for realizing smaller-size PHS. Some authors^{1,2)} reported GaAs FETs with low noise and high power characteristics, intending to integrate the front-end blocks into an RF single-chip MMIC. However, the fabrication process of these FETs seems to be slightly complicated and not cost-effective to realize the single-chip MMIC because the FETs consist of many epitaxial layers. This paper describes superior noise and power performance of the buried channel MESFET (BC-MESFET)³⁾ applicable for these applications. The BC-MESFET, which consists of one epitaxial layer on an ion-implanted channel, is more suitable for large-scale single-chip MMICs because its fabrication process could easily realize FETs with different

threshold voltage.

2. DEVICE STRUCTURE AND FABRICATION

Figure 1 shows schematic cross-sectional views of the BC-MESFET and conventional MESFET.⁴⁾ They have $0.6\text{-}\mu\text{m}$ WN_x/W -gate self-aligned asymmetric structure so that both low on-state resistance and high gate-drain breakdown voltage can be achieved. The BC-MESFET has an undoped i-GaAs epitaxial surface layer on an ion-implanted channel. The surface layer is grown by MOVPE technique after capless-annealing to activate implanted dopants and remove implantation-induced surface defects of the ion-implanted channel. Details of the process have been described in Ref. 3.

3. DC CHARACTERISTICS

The undoped surface layer contributes to enhancing breakdown voltage which is important for highly-efficient power operation. Figure 2 shows gate-drain breakdown voltage of the BC-MESFETs as a function of threshold voltage. The breakdown voltage increases with increasing surface layer thickness. The breakdown voltage for the BC-MESFET with

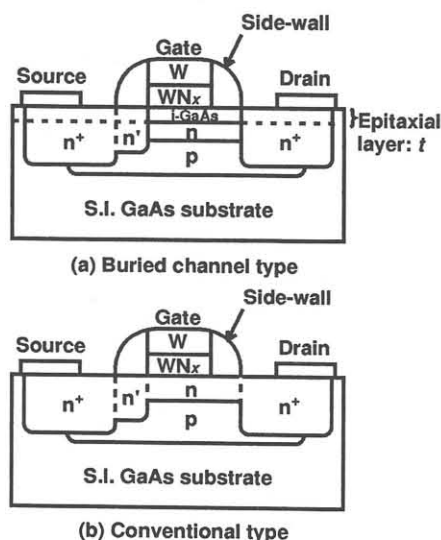


Fig. 1. Schematic cross-sectional views of the BC-MESFET and conventional MESFET.

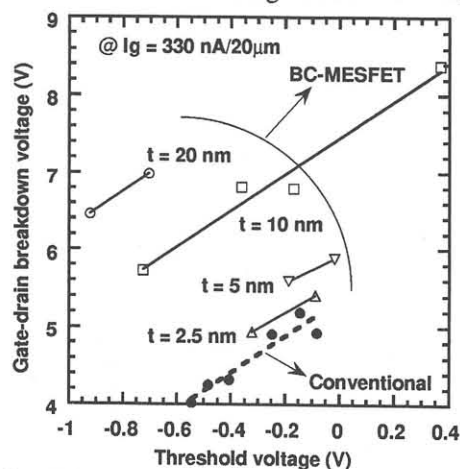


Fig. 2. Gate-drain breakdown voltage as a function of threshold voltage.

20-nm-thick surface layer is more than 3 V higher than that for the conventional MESFET. There has to be a trade-off between the breakdown voltage and controllability of threshold voltage (V_{th}) in the BC-MESFET, because thicker surface layer (t) leads to larger threshold-voltage dependence on an ion-implantation dosage (Q) into the channel as shown in the following equation

$$V_{th} = \phi_b - \frac{q}{\epsilon} \eta Q(t + t_0)$$

where ϕ_b is the Schottky barrier height, q the elementary charge, ϵ the dielectric constant of GaAs, η the activation efficiency of the implanted silicon atoms, and t_0 the constant related to acceleration energy of the ion-implantation. Thus, we have chosen the surface layer thickness of 20 nm so that the stable threshold voltage can be achieved.

Figure 3 shows the transconductance (g_m) as a function of gate voltage (V_g) for the BC-MESFET with 20-nm thick surface layer, together with the conventional MESFET which have almost the same threshold voltage. Although the peak value of the transconductance is smaller for the BC-MESFET, the transconductance is almost equal or larger below the gate voltage of -0.2 V ($V_g - V_{th} < 0.5$ V), where low noise FETs will be operated. Therefore, the superior microwave performance should be obtained in this gate-bias range since the gate capacitance (C_{gs}) is inherently smaller for the BC-MESFET because of its buried channel structure.

4. POWER PERFORMANCE

Figure 4 shows the output power and power added efficiency for a power BC-MESFET ($W_g = 1$ mm) with 20-nm-thick surface layer as a function of the input power at 1.9 GHz. We have measured these data using automated tuner system at a drain bias voltage of 2.7 V and a gate voltage of -0.5 V so as to obtain the maximum output power at around 1-

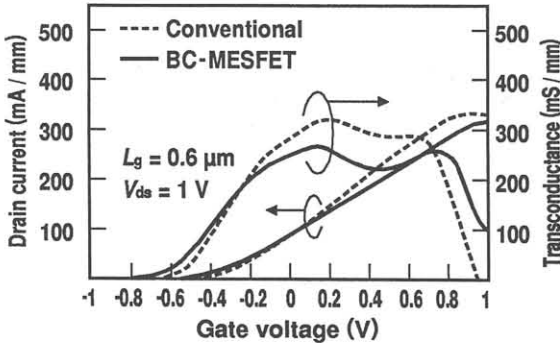


Fig. 3. Transconductance and drain current of the BC-MESFET and conventional MESFET as a function of gate voltage.

dB gain compression. An output power of 19.2 dBm and power added efficiency of 57 % are obtained at a gain compression of 1 dB and a drain current of 53 mA. These values are sufficient for the application of a highly-efficient linear power amplifier block in the PHS with long battery lifetime. Figure 5 shows the output power and power added efficiency at 1-dB gain compression as a function of incremental gate bias voltage from threshold voltage ($V_g - V_{th}$) for the BC-MESFET with 20-nm-thick surface layer and the conventional MESFET. Larger power added efficiency is obtained for the BC-MESFET than that for the conventional MESFET. The efficiency shows the peak near the $V_g - V_{th} = 0.2$ V, where these power FETs are driven under class AB condition. The improvement of efficiency for the BC-MESFET could be attributed to higher gate-drain breakdown voltage of the BC-MESFET.

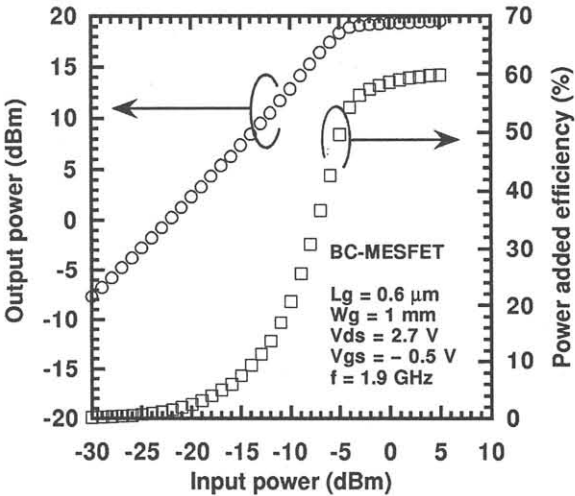


Fig. 4. Input-output characteristics of the power BC-MESFET.

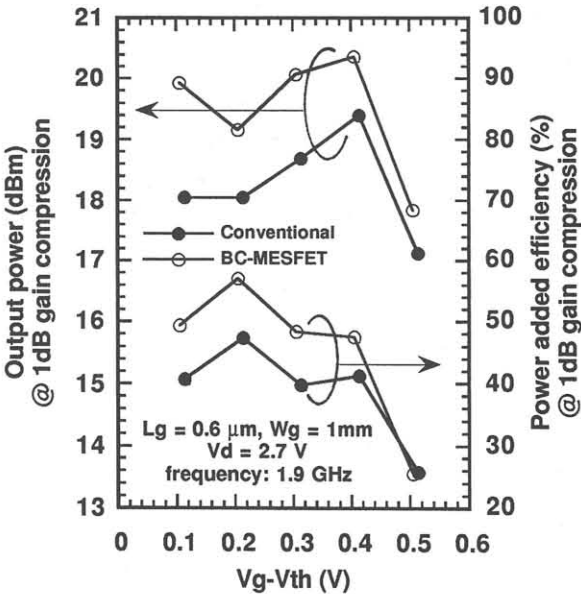


Fig. 5. Output power and power added efficiency at 1-dB gain compression as a function of incremental gate bias voltage from threshold voltage.

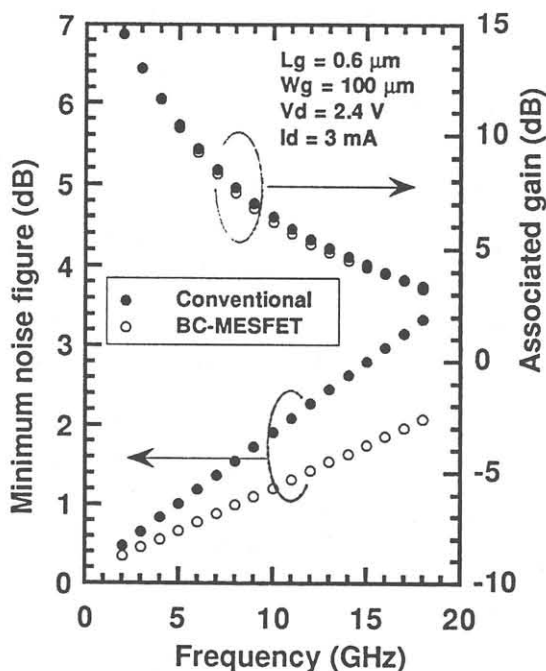


Fig. 6. Minimum noise figure and associated gain of the BC-MESFET and conventional MESFET as a function of frequency.

5. NOISE PERFORMANCE

Low noise performance should also be required to integrate the reception block into the single-chip front-end MMIC. Figure 6 shows minimum noise figure and associated gain for the BC-MESFETs with 20-nm-thick surface layer as a function of frequency. The values of conventional MESFET are also shown for comparison. In the measurement, the dissipated drain current is 3 mA ($V_g = -0.48$ V) for a gate width of 100 μm . We have obtained a minimum noise figure of below 0.4 dB and an associated gain of 14.6 dB at 2 GHz for the BC-MESFET. These values are sufficient for the reception-block application in the PHS. It can be noted that a minimum noise figure of 1.43 dB at 12 GHz is obtained for the BC-MESFETs in spite of long gate length of 0.6 μm . This value is 0.8-dB smaller than that for the conventional MESFET and close to the value for other epitaxial-channel FETs⁵⁾ with comparable gate length.

The improvement of noise figure should be attributed to the buried channel structure *i.e.* intrinsic part of the FET, because the parasitic part is almost the same between the BC-MESFET and conventional MESFET. The minimum noise figure is expressed by well-known Fukui's equation or, in case of small source and gate resistance, the equation as follows:

$$F_{\min} \cong 1 + \frac{4\pi f C_{gs}}{g_m} \sqrt{PR(1-C^2)}$$

where P and R are dimensionless parameters related to noise

current sources and C is the correlation coefficient between the gate and drain noise sources.⁶⁾ As mentioned before, the BC-MESFET has comparable value of g_m at the gate bias range of $V_g - V_{th} < 0.5$ V, where the noise measurement was carried out. Furthermore, the BC-MESFET has smaller value of C_{gs} than the conventional MESFET because the depletion layer is thicker. The calculated value of C_{gs} for the BC-MESFET was 56 fF / 100 μm , while that for the conventional MESFET was 94 fF / 100 μm . Thus, the lower noise figure should be obtained in the above equation. We have also calculated the correlation parameter of C and obtained $C = 0.72$ for the conventional MESFET and $C = 0.83$ for the BC-MESFET as typical values. Therefore, the noise reduction in the BC-MESFET could be partly originated in the cancellation effect between drain noise current and induced gate noise current.

6. CONCLUSION

The power and noise performance of the BC-MESFET has been successfully demonstrated. In spite of its simple structure, the BC-MESFET shows both high power efficiency and low minimum noise figure, which are superior to the conventional MESFET. The BC-MESFET will be one of the most promising candidates for realizing single-chip MMICs that integrate transmission and reception blocks in the PHS.

ACKNOWLEDGMENTS

The authors wish to thank Dr. T. Arikado. They would also like to thank T. Matsunaga, K. Ishida, and Y. Kuriyama for their various technical contributions.

REFERENCES

- 1) M. Sawada, E. Fujii, S. Matsushita, S. Terada, D. Inoue, H. Nakamoto and Y. Harada: Jpn. J. Appl. Phys. 34 (1995) 1168.
- 2) J. V. DiLorenzo: 1994 IEEE MTT-S Digest, p.1279.
- 3) K. Nishihori, Y. Kitaura, M. Nagaoka, Y. Tanabe, M. Mihara, M. Yoshimura, M. Hirose and N. Naotaka: Jpn. J. Appl. Phys. 34 (1995) 1241.
- 4) M. Nagaoka, K. Ishida, T. Matsunaga, K. Nishihori, T. Hashimoto, M. Yoshimura, Y. Tanabe, M. Mihara, Y. Kitaura and N. Uchitomi: Jpn. J. Appl. Phys. 33 (1994) 767.
- 5) S. Nakajima, K. Otake, N. Shiga, N. Kuwata, K. Matsuzaki, T. Sekiguchi and H. Hayashi: IEEE Trans. Electron Devices ED-39 (1992) 771.
- 6) A. Cappy: IEEE Trans. Microwave Theory Tech., MTT -36 (1988) 1.