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0.86eV Platinum Schottky Barrier on Indium Phosphide by In-Situ Electrochemical Process and Its Application to MESFETs

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Pt Schottky barrier diodes (SBDs) with Schottky barrier heights larger than 0.8eV and the ideality factor of near unity were successfully realized by a novel in-situ electrochemical process. Applying this novel technique to InP MESFETs, good gate control of drain current and enhancement-mode operation were achieved. The effective channel mobility of 1550$cm^2V^{-1}s^{-1}$ was obtained.

1.INTRODUCTION

High speed InP Schottky barrier diodes (SBDs) and metal semiconductor field effect transistors (MESFETs) are potentially useful for applications in InP-based monolithic optoelectronic integrated circuits (OEICs). However, realization of such devices have so far been difficult because direct metal contact formation on InP by conventional techniques results in low Schottky barrier heights (SBHs) of about 0.4 eV, being independent of metal workfunctions due to the so-called Fermi level pinning.

To overcome this, many investigations were performed for n-InP SBDs. Most of them were realized by the incorporation of thin oxide layer [1,2] or p^+ planar-doping layer[3] in the metal/InP interface in order to enhance the SBH. However, SBDs with various oxide layers were suffered from instability and poor reproducibility due to the complex interfacial reactions.[4] In addition, MESFETs utilizing Schottky gate having interlayers generally exhibit current fluctuation, kinks and poor pinch-off.[5-7]

In this respect, we have shown recently that InP Schottky barriers produced by our novel in-situ electrochemical process are free of interfacial oxides and near-surface deep traps and removes Fermi level pinning, realizing workfunction-dependent SBHs.[8]

The purpose of this paper is to demonstrate that Pt SBDs and Pt gate MESFETs with SBH larger than 0.8eV can be reproducibly realized on InP by this novel electrochemical process

2.EXPERIMENTAL

The experimental set-up is shown in **Fig.1(a)**. The in-situ electrochemical process consists of anodic etching and subsequent Pt deposition in the same electrolyte (H_2Cl_6Pt). The set-up possesses three electrodes, including an InP substrate, a Pt counterelectrode and a reference saturated calomel electrode (SCE). The InP electrode was fixed with wax to the sample holder and connected electrically to the outer circuit. **Fig.1(b)** shows the electric pulse waveforms for avalanche pulse etching and pulse plating, respectively. The potential of the InP electrode was controlled by a potentiostat with a pulse generator. The pulse generator provides voltage pulses for the avalanche pulse etching and pulse plating. After several hundreds Å thick InP was etched by the avalanche pulse-assisted anodic dissolution, Pt was immediately deposited in-situ by pulse plating on the etched InP surface. Pulse plating was found to improve the current efficiency of Pt deposition, avoiding H_2 evolution at the Pt surface which is usually a problem in DC plating.[9]

For SBD samples, n-type InP substrates with a carrier concentration of $n=5x10^{15}cm^{-3}$ were used. For ohmic electrodes, GeAu/Ni contact layer was evaporated on the backside of substrate and annealed in H_2 for 5 minutes at a temperature of 350°C. InP surfaces were masked by photoresist to define the circular areas of the diodes. The area of the diodes were $2.3x10^{-3}cm^2$.

For InP MESFETs, epitaxial layers were grown by gas-source MBE using In and tertiarybutylphosphin (TBP) on Fe-doped semi-insulating InP substrates. The carrier

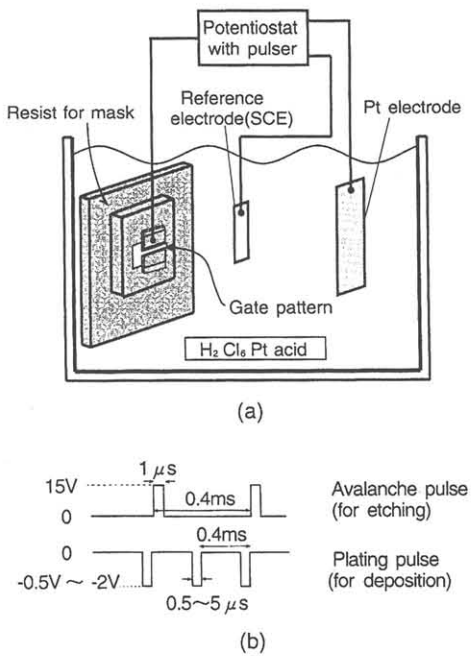


Fig. 1 Set-up of electrochemical process and pulse forms for etching and plating

concentration and mobility of epitaxial layers determined by Hall measurement were $3x10^{16}$-$1x10^{17}cm^{-3}$ and 1,100-2,700$cm^2V^{-1}s^{-1}$, respectively. The fabrication process of MESFET was the following. Source and drain ohmic contacts were formed on mesa-etched islands of InP epitaxial layers. The gate was defined with rectangular opening in a photoresist layer and formed by Pt plating. The current-voltage (I-V) characteristics were measured by HP4156A semiconductor parameter analyzer.

3. RESULTS and DISCUSSION

3.1 Pt/n-InP SBDs

Figure 2 compares the I-V curves of Pt/n-InP SBDs prepared by the electrochemical process and by conventional electron beam (EB) deposition. The novel process achieved an extremely high SBH of 0.86eV and the ideality factor of 1.17, whereas the EB process yielded a conventional SBH of 0.44eV. The difference in leakage currents between electrochemical and EB diodes was as large as 5 orders of magnitude at the reverse bias of -2V.

In order to investigate interface properties of Pt/n-InP SBDs, capacitance-voltage (C-V) measurement was performed. As compared with interlayer-modified InP SBDs to enhance SBH, the present diodes were extremely well behaved as can be seen in **Fig.3**. The $1/C^2$-V curve shows an excellent linearity and a built-in potential as high as 0.72eV that corresponds to SBH of 0.84eV. Some of the measured values of SBH by I-V ($\phi^{I\text{-}V}_{Bn}$) and C-V ($\phi^{C\text{-}V}_{Bn}$) methods and ideality factor n are summarized in Table 1. $\phi^{I\text{-}V}_{Bn}$ are in good agreement with $\phi^{C\text{-}V}_{Bn}$ and values of n was near unity. Previous X-ray photoelectron spectroscopy (XPS) analysis [8] showed that there were no oxide phases at the Pt/InP interface formed by the novel process. These results indicate that nearly ideal Schottky barriers without interfacial oxides and near-surface damages can be produced by the present process.

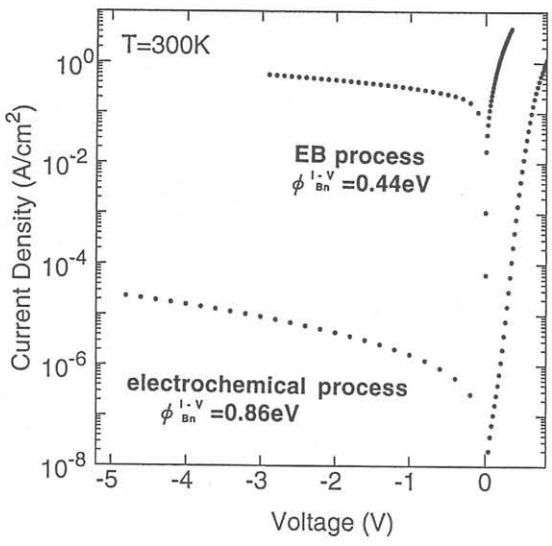


Fig. 2 Reverse I-V curves of Pt/n-InP diodes

3.2 MESFET Characteristics

The novel in-situ process enables selective gate metal deposition by using photoresist as the mask. As an example, a SEM micrograph of a fabricated InP MESFET with 2.5-μm Pt gate is shown in **Fig.4**. Pt is homogeneously plated with smooth edges following the gate pattern. Separate experiments have shown that such uniform deposition can be made in the submicron range using EB lithography.[10]

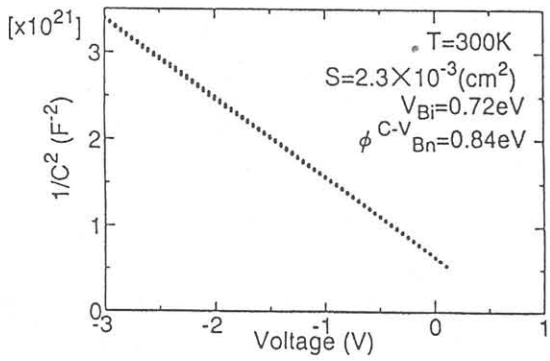


Fig. 3 C-V curves of Pt(electrochemical)/n-InP diode

Table 1:Summary of SBHs and ideal factor of Pt/n-InP diodes by the novel process

samples	$\phi^{I\text{-}V}$(eV)	$\phi^{C\text{-}V}$(eV)	n-value
a	0.87	0.84	1.19
b	0.80	0.86	1.16
c	0.81	0.85	1.17
d	0.88	0.80	1.15

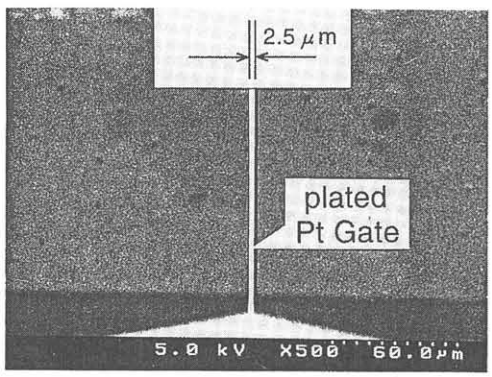
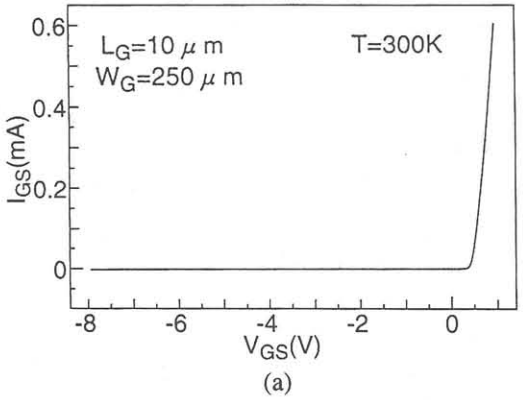
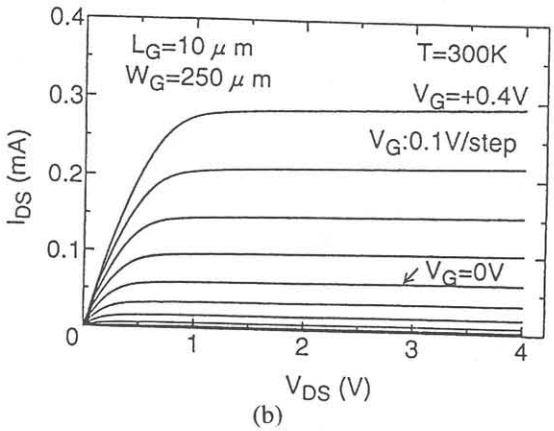


Fig. 4 SEM photograph of MESFET after gate plating

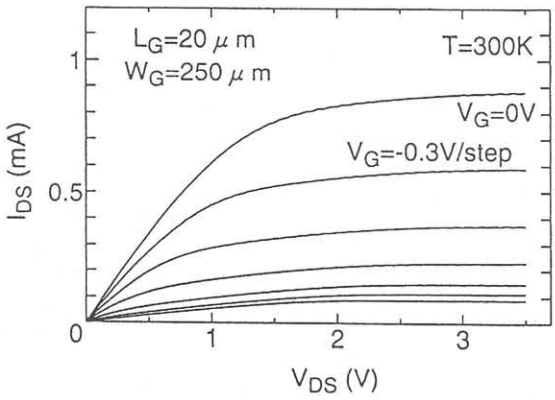


(a)

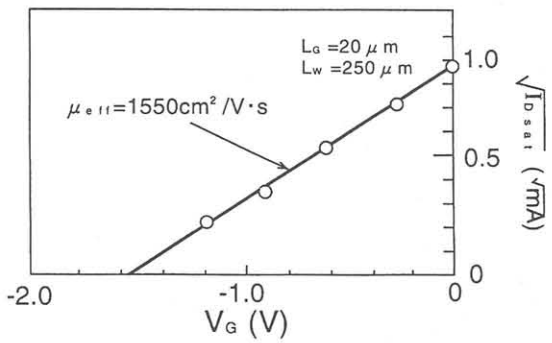


(b)

Fig. 5(a) Gate I-V curve of InP MESFET
(b) Drain I-V characteristics with positive gate bias application for InP MESFET



(a)



(b)

Fig. 6(a)Drain I-V characteristics for InP MESFET
(b) Square root of the drain saturation current vs. V_G

Fig.5(a) shows typical gate I-V curve of the device having the channel thickness of 1200Å. Turn-on voltage over 0.6V and reverse leakage current lower than 1μA at Vg=-5V were obtained, indicating excellent gate characteristics with higher SBH. Because of such a high SBH, enhancement MESFETs can be realized with this technology. The drain I-V characteristics of the device is shown in **Fig.5(b)**. Good gate control of drain currents was achieved even under the positive gate bias and the devices gave perfect pinch-off. Such devices may be useful for construction of DCFL circuits on InP-based OEICs.

Drain I-V characteristics of a depletion mode InP MESFET are shown in **Fig.6(a)**. The channel thickness was about 3500Å and carrier concentration was $3.0x10^{16}cm^{-3}$. Square root of the drain saturation current is plotted vs. gate voltage in **Fig.6(b)**, and its slope gives a value of the effective electron mobility of 1,550 $cm^2V^{-1}s^{-1}$. This is very close to the Hall effect mobility of the epitaxial layer.

4.CONCLUSION

Pt Schottky barrier diodes (SBDs) with Schottky barrier heights larger than 0.8eV and the ideality factor of near unity were successfully realized by our novel in-situ electrochemical process. Applying this novel technique to InP MESFETs, good gate control of drain current and enhancement-mode operation were achieved. The effective channel mobility of $1550cm^2V^{-1}s^{-1}$ was obtained. Such devices may be useful for construction of DCFL circuits on InP-based OEICs

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