Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 1081-1082

LB-L10

InP-Based High-Performance Monostable-Bistable Transition Logic elements (MOBILEs) Using Resonant-Tunneling Devices

Kevin J. Chen, Koichi Maezawa, and Masafumi Yamamoto
NTT LSI Laboratories, 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan
Telephone: +81 462 40 2612 Fax: +81 462 40 2872

We have recently proposed and demonstrated a highly functional logic gate called MOBILE [1] (Monostable-Bistable Transition Logic Element) which employs resonant-tunneling devices. A more practical approach to building devices suitable for MOBILE circuits has also been demonstrated in the AlGaAs/GaAs material system based on the monolithic integration of resonant-tunneling diodes (RTDs) and FETs [2,3]. On the other hand, the ultimate performance (speed and operating margins) of MOBILE's requires: 1) high peak current density, 2) high peak-to-valley (P/V) ratio, and 3) high transconductance of the FETs integrated with RTDs. InP-based material system emerges as the optimum material choice, since both RTDs and FETs have shown superior characteristics in InP. In this study, we report the first InP-based MOBILE.

The concept of MOBILE has two aspects (see details in Ref. [1]): 1) employing the monostable-to-bistable transition of a circuit consisting of two RTT's connected in series, and 2) driving the circuit by periodic variation of the bias voltage (V_{bias}). A small difference in the peak currents between the driver and load device determines the circuit's state after transition. Our approach to generating this difference in peak currents is to modulate the peak current of the RTTs through an FET (HEMT in this case) gate, which is integrated with an RTD in parallel.

Figure 1 shows the cross section and the MBE-grown epitaxial structure of the integrated RTD/HEMT pair. The gate voltage modulates the current through the HEMT channel (I_{HEMT}), which results in the modulation of the total source-to-drain current $I_{DS}(=I_{RTD}+I_{HEMT})$. The RTD uses a InGaAs/AlAs/InAs pseudomorphic structure, in which a strained InAs layer is inserted in the quantum well to effectively reduce the peak voltage. A heavily doped InAlAs selective etch-stop layer is grown just above the HEMT structure to improve the uniformity of the threshold voltage and transconductances of the HEMT's which are critical to the accurate operations in multiple-input (multiple-gate) MOBILE logic circuits.

On the same wafer, RTDs exhibit a P/V ratio of 5.5:1 at room temperature, with a peak current density of 85 kA/cm^2. HEMT's have a maximum transconductance of 850 mS/mm for 0.7 μm-gate devices. These characteristics are comparable to those shown in the state-of-the-art RTD's and FET's. Figure 2 shows the current-voltage characteristics of an integrated device. The peak current is clearly modulated by the gate voltage.

To demonstrate the MOBILE operation, an inverter operation together with the circuit configuration is shown in Fig. 3. The load RTD is intentionally designed to have a larger area (larger peak current) than that of the driver RTD. When the input signal is 0 V (logic "0"), the larger load peak current leads to logic high in output. When input is 0.5 V (logic "1"), driver peak current becomes higher than that of the load, and the output becomes logic low.

One of the most important functions of MOBILEs is the weighted sum threshold logic operation [4]. Figure 4 shows the circuit configuration and timing diagram of a fabricated MOBILE with three-input gates and a 1:2:4 width ratio. All 8 (2^3) input patterns of the weighted sum can be distinguished by selecting the threshold value via the control gate bias with improved operating margin attributed to the high P/V ratio in the RTDs and uniformity in the HEMTs' characteristics. A higher operating speed is also expected from the high current density of the RTDs on InP.

In summary, we have demonstrated the first InP-based MOBILEs with characteristics suitable for high performance operations.

[1] K. Maezawa, and T. Mizutani, *Jpn. J. Appl. Phys.* vol. 32 (1993), p. L42.
[2] K. J. Chen, T. Akeyoshi, and K. Maezawa, *IEEE Electron Device Lett.*, vol. 16 (1995), p. 70.
[3] K. J. Chen, T. Akeyoshi, and K. Maezawa, *Jpn. J. Appl. Phys., vol.* 34 (1995), p. 1199.
[4] T. Akeyoshi, K. Maezawa, and T. Mizutani, *IEEE Electron Device Lett.*, vol. 14 (1993), p.475.

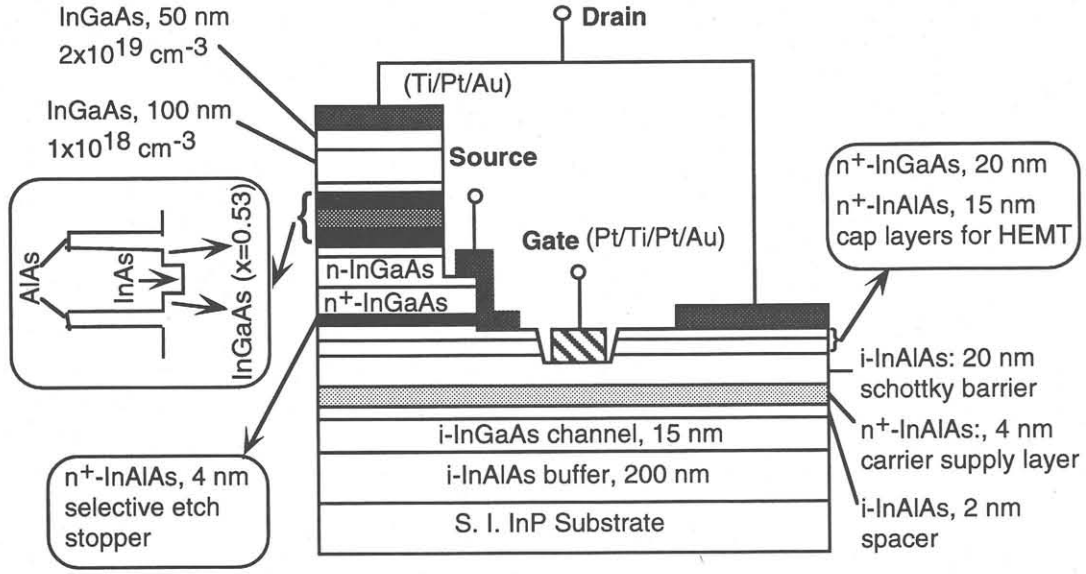


Fig. 1 Schematic cross section of the integrated device. The cathode of the RTD and the source of the HEMT are connected. The anode of the RTD and the drain of the HEMT are connected.

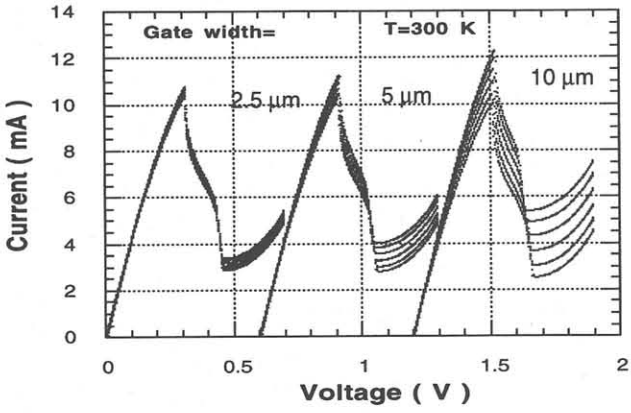
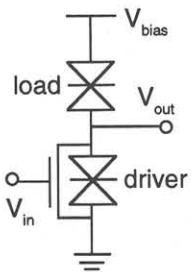


Fig. 2 I-V characteristics of an integrated device, in which one RTD is in parallel with three HEMTs with 1:2:4 gate width ratio. Gate length is 0.7 μm. The modulation of the peak current is proportional to the gate width. The curves for 5mm- and 10mm-gate are shifted from the origin by 0.6 V and 1.2 V, respectively.



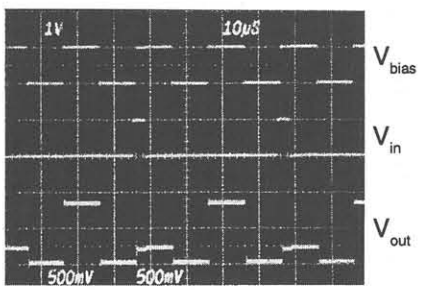
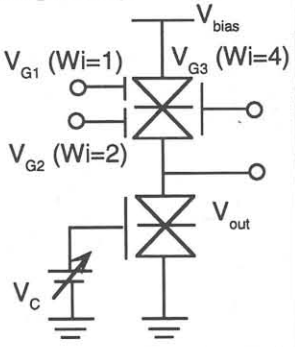


Fig. 3 The inverter operation of a MOBILE gate.



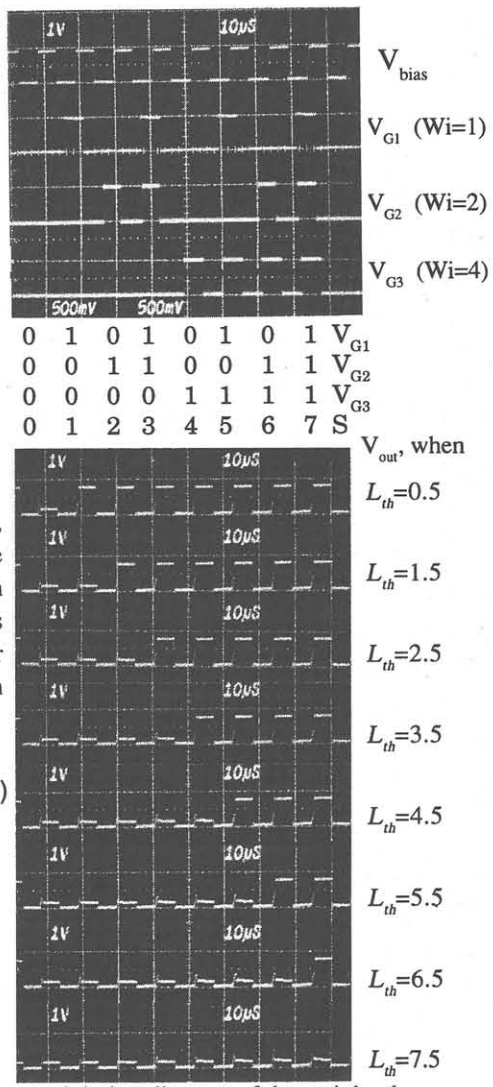


Fig. 4 Circuit configuration and timing diagram of the weighted sum threshold operation. $V_{out}=u(y)$, where u is step function and $y=S-L_{th}$, $S(=\Sigma W_i X_i)$ is the weighted sum, and X_i and W_i are the input signal and the weight of the i_{th} input. L_{th} is the threshold which can be selected from 0.5 to 7.5 by changing V_C.