Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 1071-1072

Ultra-Thin Fatigue Free $Bi_4Ti_3O_{12}$ Thin Films for Nonvolatile Ferroelectric Memories

T.Kijima, S.Satoh, H.Matsunaga and M.Koba
Functional Devices Laboratory, SHARP Corporation
273-1 Kashiwa, Kashiwa-shi, Chiba 277, Japan

Abstract

This paper describes the MOCVD method to form $Bi_4Ti_3O_{12}$ (abbreviated as BIT) thin films with enough electrical properties for nonvolatile ferroelectric memories (NVFRAMs). We have developed a new low temperature growth technique, in which ultra-thin double buffer layer (5nm-BIT/5nm-TiO_2) was used to control the crystallization and fine grain structure of BIT thin films. It has been achieved that 100nm-BIT thin films fabricated at 400℃ showed an excellent smooth surface morphology and good electrical properties; large remanent polarization of Pr=11 μ C/cm^2, coercive field of Ec=90kV/cm and low leakage current I_L=7×10^{-9} A/cm^2 at 3V, respectively. Besides, for the first time the fatigue free property, which was very important for NVFRAMs applications, was confirmed up to 1×10^{12} switching cycles.

Introduction

Recently, BIT thin film preparation has been investigated to use the ferroelectrical applications for NVFRAMs by MOCVD method[1,2]. BIT crystals have a typical layered perovskite structure and show strong anisotropic properties; Pr of 50 and 4 μ C/cm^2 along the a- and c-axis, respectively. Therefore, the a-axis component of large Pr is advantageous to reduce a memory cell area. On the other hand, a low temperature film formation process is desired for the realization of poly-Si plug stacked capacitor (PSC) memory cell[3]. Because, the inter-diffusion phenomena between electrode and poly-Si plug happens during ferroelectric film formation at high temperature. However, up to the present, it has been necessary high deposition temperature (>600℃) in order to obtain the single phase BIT thin films. Besides, it was reported that the prepared BIT films (280nm-thick) showed the c-axis orientation and poor ferroelectric properties of Pr=1.3 μ C/cm^2 and Ec=25kV/cm[1].

Experimental

BIT films were deposited on a 6-inch diameter Pt-coated Si wafer substrate using an equipment and BIT film deposition conditions as shown in Fig. 1 and Table 1. We proposed a new sequence of film formation process, which temperature profile and schematic film structure are shown in Fig. 2. In step 1, in order to increase of BIT nucleation density on a Pt surface, titanium oxide buffer (TB) layer with 5nm thickness was deposited at 400℃. Successively, in step 2, BIT nucleation (BN) layer with 5nm thickness was deposited on TB layer at 550℃. In the last step 3, BIT growth (BG) layer with 90nm thickness was deposited at different substrate temperatures of 400 and 550℃, respectively. In order to clarify an advantage of our new process, BIT films with no buffer layer were also prepared at deposition temperatures of 400 and 550℃.

Results and Discussion

Figure 3(a) and (b) show the surface morphology and XRD patterns of BIT films with no buffer layer deposited at 550 and 400℃. BIT film deposited at 550℃ showed the c-axis-oriented crystalline film consisted of large plate-like grains, but the BIT film deposited at 400℃ was amorphous. On the other hand, Figure 4(a) and (b) show XRD patterns of BIT films deposited at 400℃, using double buffer (BN/TB) and single buffer (TB) layers, respectively. It was clear that BIT films could be crystallized at 400℃ by using a buffer layer. Especially, the BIT film with double buffer (BN/TB) layer shows a single phase random-oriented crystalline state, which is advantageous to realize the large Pr value. However, the XRD pattern of BIT film with single buffer (TB) layer shows a coexistence of pyrochlore ($Bi_2Ti_2O_7$) phase. Therefore, double buffer (BN/TB) layer structure is essential to obtain the single phase BIT films at low temperature. The film thickness dependence of surface roughness (R_{max}) measured by AFM is shown in Fig. 5, in which solid (—) and dotted (---) lines show the BIT films with double buffer layer deposited at 400 and 550℃, respectively. The surface roughness increased with film thickness and deposition temperature. It was confirmed that the surface roughening was significantly suppressed at low temperature, which was advantageous to PSC memory cell formation process. An example of small size capacitor structure with BIT thin film is shown in Fig. 6.

Platinum upper electrodes were evaporated on the BIT films deposited at 400℃ to measure the electrical properties. Polarization hysteresis loops measured using a pulse test system (RT-66A) and leakage current density are shown in Fig. 7 and 8. Even the 100nm ultra-thin BIT film shows good electrical properties; Pr of 11 μ C/cm^2, Ec of 90kV/cm and I_L of 7×10^{-9} A/cm^2 at 3V. These properties are top data of BIT thin films reported up to now. The fatigue property was measured using bipolar pulses of 4V amplitude and of 1MHz frequency. Figure 9 shows the decay of the normalized switched polarization as a function of the number of polarization reversing switching cycles. There was only a little decay less than 3% up to 1×10^{12} cycles.

Summary

Ultra-thin BIT films with enough electrical properties for NVFRAM were fabricated for the first time using a new low temperature growth technique by MOCVD method at 400℃. Large remanent polarization of 11 μ C/cm^2 and low leakage current of 7×10^{-9} A/cm^2 at 3V were attained for the 100nm thin film. No fatigue is almost observed after 10^{12} polarization switching cycles even though a complex electrode structure is not used.

References

[1] R.Muhammet et al., J.J.A.P.33(1994)5215.
[2] K.Yoshimura et al., J.J.A.P.34(1995)2425.
[3] S.Onishi et al., IEDM Tech. Dig.,(1994)843.

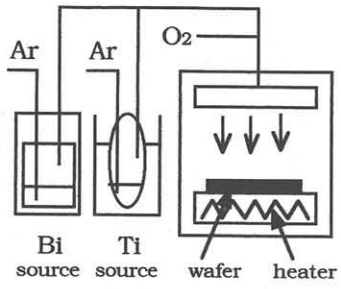

Fig.1 Schematic diagram of the apparatus for MOCVD-BIT.

Table 1 Deposition conditions of BIT films.

Precursors	$Bi(o\text{-}C_7H_7)_3$	$Ti(i\text{-}OC_3H_7)_4$
Precursors temp.	160℃	50℃
Gas flow rate		
Ar carrier gas	200sccm	50sccm
O_2 gas	1000sccm	
Pressure	5Torr	
Substrate	$Pt/Ta/SiO_2/Si(100)$	

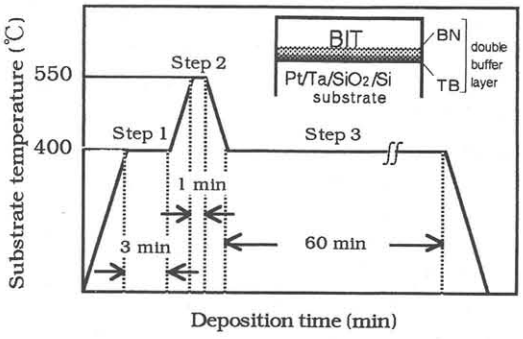

Fig.2 Temperature profile for BIT deposition and schematic film structure.

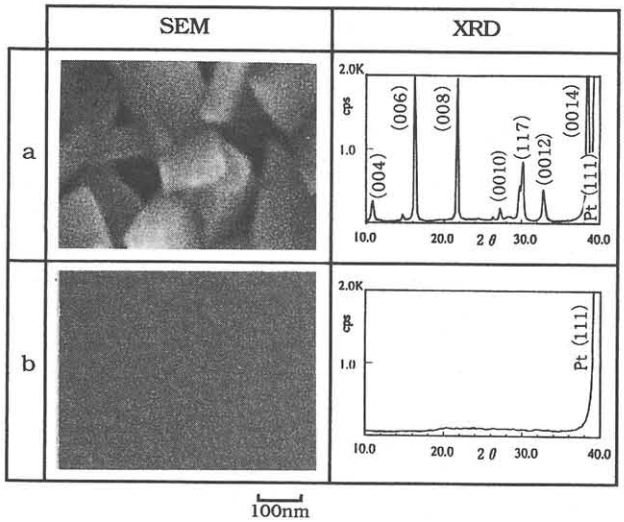

Fig.3 SEM photographs and XRD patterns of BIT films with no buffer layer deposited at (a)550 ℃ and (b)400 ℃.

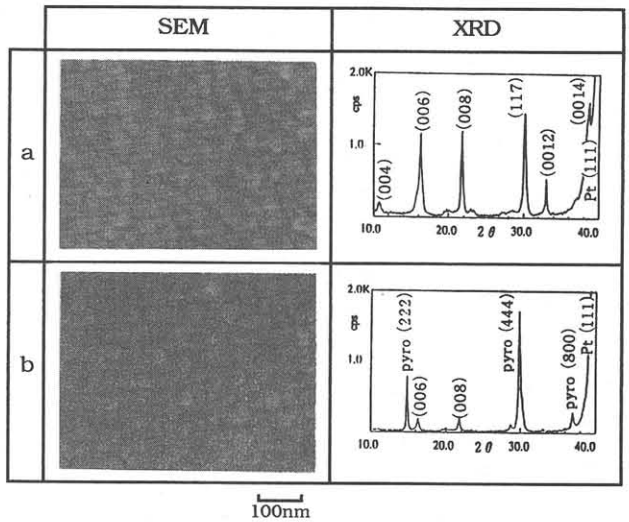

Fig.4 SEM photographs and XRD patterns of BIT films deposited at 400℃, using (a) double buffer (BN/TB) and (b) single buffer (TB) layers.

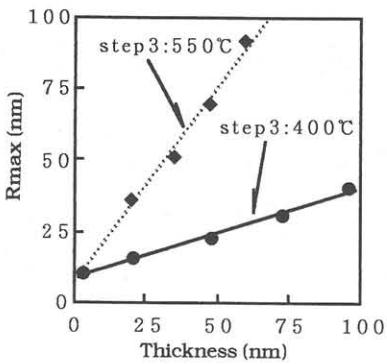

Fig.5 Dependence of surface roughness on BIT film thickness at the deposition temperatures of 400℃ and 550℃.

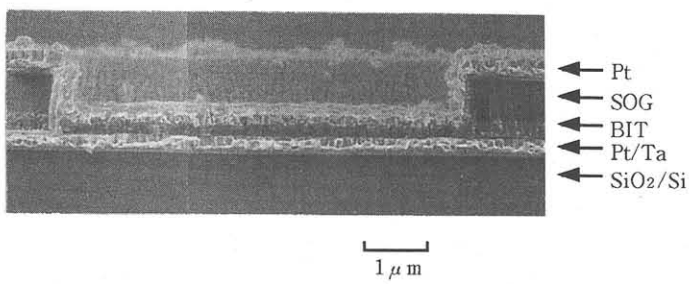

Fig.6 SEM photograph of BIT capacitor.

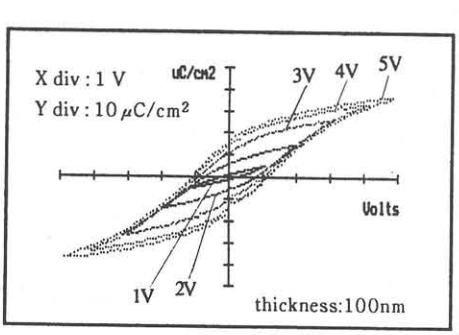

Fig.7 D-E hysteresis loops of a 100nm thick BIT film measured at 2 KHz and various applied voltage (1,2,3,4 and 5V).

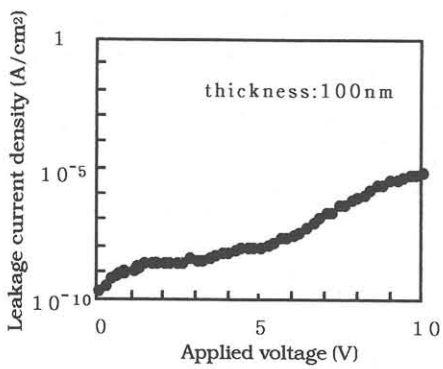

Fig.8 Leakage current characteristics of BIT thin film at room temperature.

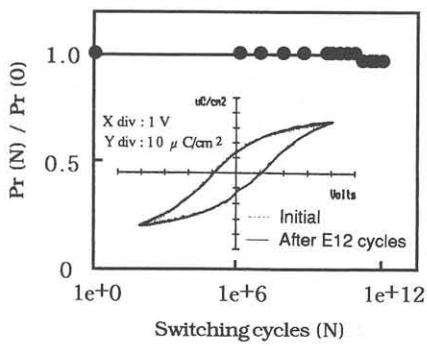

Fig.9 Normalized switched polarization as a function of switching cycles.