Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 1073-1074

Three-Diensional Integration Technology Based on Wafer Bonding Technique Using Micro-Bumps

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<Introduction> Recently, the demand to very fast image processing LSI with real time operation capability has become rapidly increasing. However, it is very difficult to achieve such LSI by using a conventional two-dimensional (2D) LSI technology because the eventual image processing speed is limited by converting 2D image data to 1D image data. Long interconnections required in 2D image processing LSI also limit the processing speed. These problems can be solved if three-dimensional (3D) LSI technology can be used for fabricating the image processing LSI because 2D image data can be treated as it is and we can use many short interconnections in the vertical direction which dramatically reduce a wiring delay. In the past, many people had tried to develop 3D LSI technology using laser annealing technique, zone melting technique, solid phase epitaxial technique and so on. However such 3D LSI technology had not been employed in production because it was very complicated and expensive technology. Then, we propose in this paper more realistic 3D LSI technology based on a wafer bonding technique using micro-bumps.

<New 3D LSI Structure> Fig.1 represents a basic configuration of 3D image processing LSI which consists of four layers of image sensor array layer, amplifier and AD converter array layer, data latch and masking circuit array layer and processor array and output circuit layer. Process sequence to fabricate such 3D image processing LSI is shown in Fig.2. 2D LSI wafer with buried interconnections is used as a starting wafer for 3D LSI. The buried interconnections are formed by depositing n^+ poly-Si into trenches which are formed through the field oxide. 2D LSI wafer with buried interconnections is glued to a quartz glass and then thinned to around 30μm by grinding and chemical-mechanical polishing. The thinned wafer is bonded to a thick wafer through micro-bumps after careful wafer alignment. UV hardening adhesive layer with thickness of 1μm is inserted between two wafers to enhance the bondability of two wafers. 3D LSI can be fabricated by repeating such sequence.

<Element Technologies for 3D LSI> Formation of buried interconnection, wafer thinning, wafer alignment and wafer bonding through micro-bumps are key element technologies for our 3D LSI. Then, these element technologies were developed and basic device characteristics on stacked wafer were evaluated. It is required to form deep silicon trench in order to form the buried interconnection. Deep silicon trench with the depth of more than 30μm can be formed by using a high speed RIE etcher with etching gas of SF_6 as shown in Figs.3 and 4. Wafer temperature was lowered to avoid the temperature rise during etching. Grinding and chemical-mechanical polishing techniques were used to thin the wafer to 30μm. We did not thin the wafer less than 30μm to avoid wafer cracking during handling although it was easy to thin to less than 30μm . Wafer thickness variation after thinning was very small as 30μm$\pm$0.5μm in 6 inch wafer as shown in Figs.5 and 6. For a wafer alignment, we have developed a new wafer aligner as shown in Fig.7. Wafer stage is precisely controlled with accuracy of 50nm in x,y,z directions by piezo actuators in this aligner. Six inch wafers can be aligned with alignment tolerance of $\pm$1μm after contacting. We can detect the infrared light signal through ten layers. The gap between two wafers are measured in-situ and precisely controlled during alignment. This aligner can also force a mechanical pressure to the wafer during bonding. In/Au micro-bumps and UV hardening adhesive layer were used to bond two wafers. The minimum micro-bump size was 5μmx5μm. Good electrical contact was obtained between two micro-bumps after bonding by optimizing the micro-bump and bonding conditions as shown in Table.1. I_D-V_D characteristics of MOS transistor formed on stacked wafers are shown in Fig.8.

<Conclusions> A new 3D LSI technology has been proposed. Several element technologies such as deep trench formation for buried interconnection, wafer grinding and chemical-mechanical polishing, wafer aligning and wafer bonding with micro-bumps have been developed for this 3D LSI.

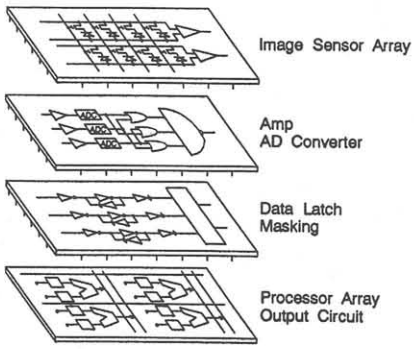


Fig.1 Real time image processor with 3D strucure.

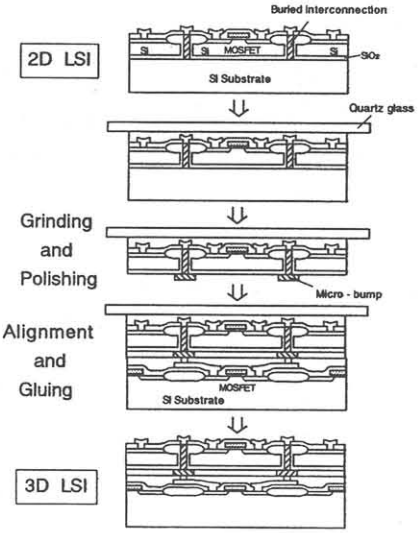


Fig.2 Fabrication sequence of 3D LSI.

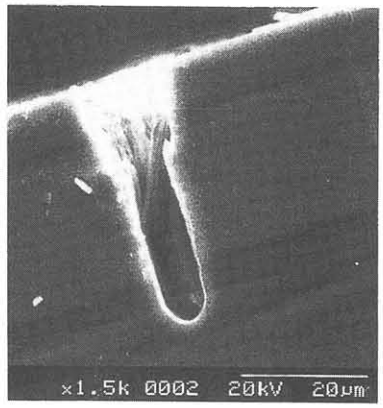


Fig.3 SEM cross-section of deep silicon trench.

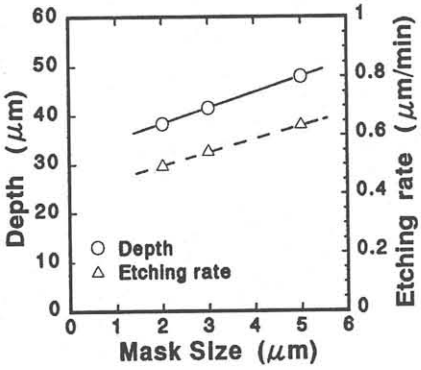


Fig.4 Trench depth and etching rate as a function of trench width.

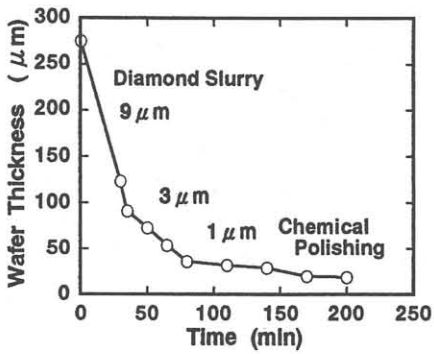


Fig.5 Wafer thickness after grinding and chemical-mechanical polishing.

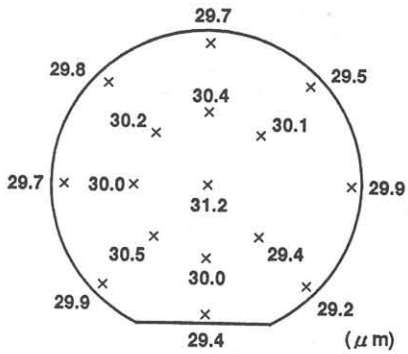
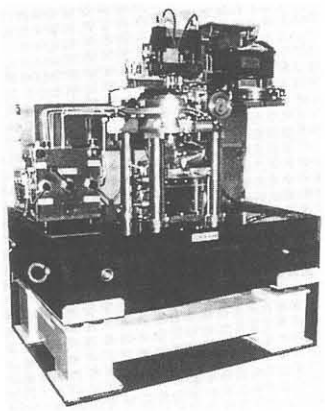
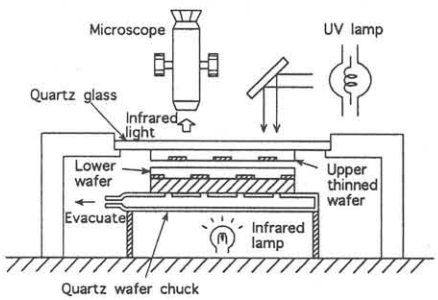


Fig.6 Thickness variation in 6 inch wafer after thinning.



(a)



(b)

Fig.7 Photograph of 3D wafer aligner.

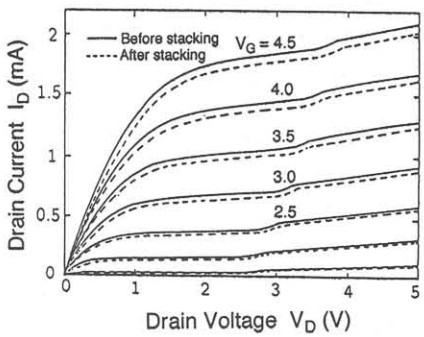


Fig.8 I_D-V_D characteristics of MOS transistor formed on stacked wafers.

		A	B	C	D	E	F
Bump Thickness Au / In (nm / nm)	Upper Bump	100/900	100/900	500/500	500/500	100/900	100/900
	Lower Bump	100/900	100/900	500/500	500/500	500/500	500/500
Soldering Temperature(℃)		150	90	90	150	150	150
Soldering Time (minute)		1	30	30	5	5	1
Contact Resistance		○	○	×	×	○	○

Table.1 Measurement results of micro-bump contact resistance.