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Optically Interconnected Kohonen Net for Pattern Recognition

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1. Introduction

A unique feature of optical interconnection for integrated systems is free from the parasitic capacitance, and hence the signal transfer speed is independent of the fan-out numbers [1]. This implies that the optical interconnection is well suited for data bus lines or clock distributions to a large number of processing elements. Kohonen net which implements pattern recognition [2] needs massive data distributions which can be realized by optical waveguides as schematically shown in Fig. 1. Here, the input pattern data are distributed to many processors in which the distance between the input and the reference patterns is simultaneously calculated to obtain the minimum distance for pattern recognition. So far a few studies on optoelectronic microsystems consisting of optical waveguides, photodiodes and CMOS circuits have been reported and the size of the Y-shaped branch waveguide was as large as ~1 mm [3,4].

We have newly developed compact bent waveguides and branched waveguides capped with an Al layer. These optical components and photodiodes have been monolithically integrated on a single Si wafer together with CMOS chips to fabricate Kohonen net, and the fundamental operation of the pattern recognition has been demonstrated.

2. Test chip fabrication

The layout of optical waveguides, photodetectors and CMOS circuits integrated on a Si wafer is schematically shown in Fig. 2. The right-angle branched waveguides and newly developed corner bent waveguides were fabricated on the Si wafer. The eight branch waveguides (total length: 40 mm) were connected to the n^+/p photodiodes. The 2 μm CMOS chips were bonded to the Si wafer and connected with the photodetectors by Au wire bonding technique. The photograph of the fabricated test chip is shown in Fig. 3. The cross section of the test chip is also shown in Fig. 4, where the waveguides and n^+/p junction photodiodes were fabricated with the CMOS compatible process. The curved Si surfaces prepared by the wet chemical etching was used for micromirrors to introduce the incident light to the waveguide [5,6]. Then photodiodes were fabricated by As^+ ion implantation after LOCOS process. Next, the SiO_2 film was deposited by atmospheric pressure CVD at 450°C as a bottom cladding layer. The Si_3N_4 film was subsequently deposited at 750° C by low pressure CVD (LPCVD) as a core layer. The double layer was patterned with electron beam lithography in which the edge of the resist mask was tapered by the back scattering of electrons using intentional excess dose as illustrated in Fig. 5. By dry etching of the nitride and oxide layer with the tapered resist mask, the double layer was taper etched to fabricate the micromirrors. Finally a top cladding SiO_2 layer was deposited by LPCVD, and the waveguides were covered with an Al layer so as to fabricate micromirrors and to significantly reduce the light propagation loss [5].

3. Test chip performance

A measurement circuit for testing the fabricated chip is shown in Fig. 6. The signal light is introduced to the waveguide from a semiconductor laser through an optical fiber and propagates to the photodiode. The photocurrent flows into a resistance connected to the photodiode, resulting in the decrease of the photodiode output signal. When the laser light is on, signal "0" is applied to the input electrode of the XOR circuit. This circuit calculates one bit distance between the input signal and the reference one (always "1" in the present case). When the optical input signal is equal to the reference signal, the output is "0", while it is "1" when they do not coincide.

The input signal to the semiconductor laser and the output waveform from the XOR circuits are displayed in Fig. 7 (a) and (b), respectively, showing that the circuit is operating at a frequency of 6.7 MHz. A delay time of the XOR circuit is evaluated to be about 100 ns. There is a parasitic capacitance of about 5 pF connected in parallel to the photodiode. Since the resistance of 10 kΩ is connected in series with this capacitance as illustrated in Fig. 6, the RC time constant becomes about 50 ns, which limits the operation speed of the test circuits. In this hybrid integrated circuits, the parasitic capacitance is dominantly determined by the capacitance of the bonding pad. Therefore, the operation speed of the Kohonen net is expected to be ten times faster than that of the present circuits by integrating the CMOS circuits and photodiodes on a single chip.

4. Summary

We have designed and fabricated the test chip of Kohonen net which implements the pattern recognition. The Kohonen net consists of CMOS chips bonded onto the Si wafer on which the optical waveguides, photodiodes and micromirrors are monolithically integrated.

References

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[6] T. Nagata, T.Tanaka, K.Miyake, H. Kurotaki, S. Yokoyama, M. Koyanagi, Jpn. J. Appl. Phys. **33** (1994) 822.

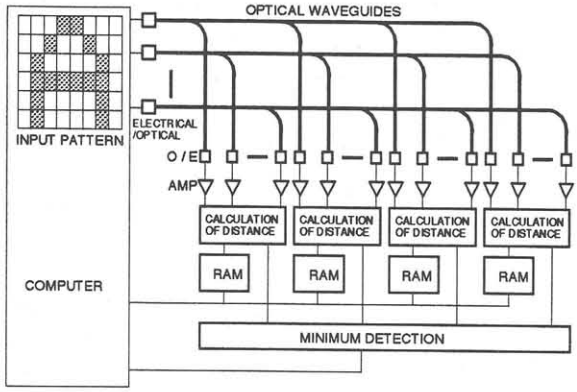

Fig. 1 Optically interconnected Kohonen net.

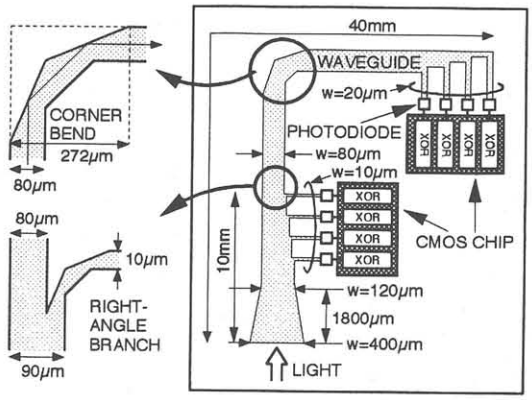

Fig.2 Schematic view of a fabricated test chip.

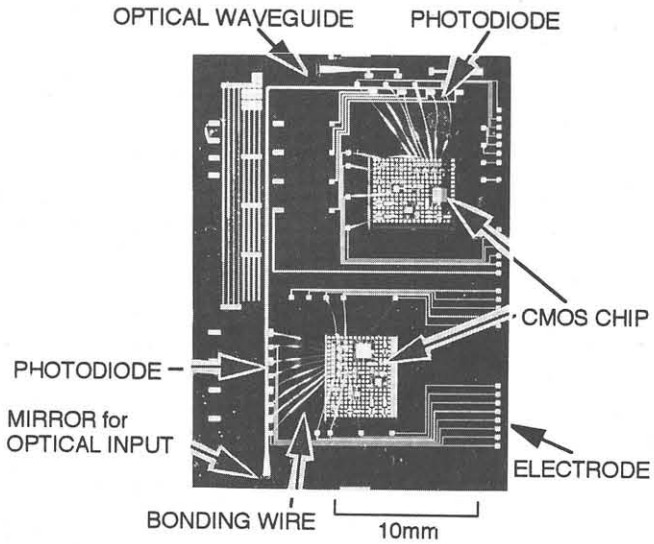

Fig. 3 Photograph of a test chip.

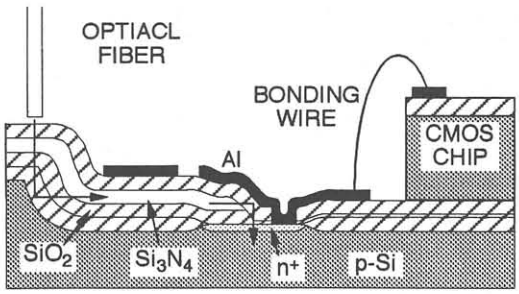

Fig. 4 Cross section of a test chip.

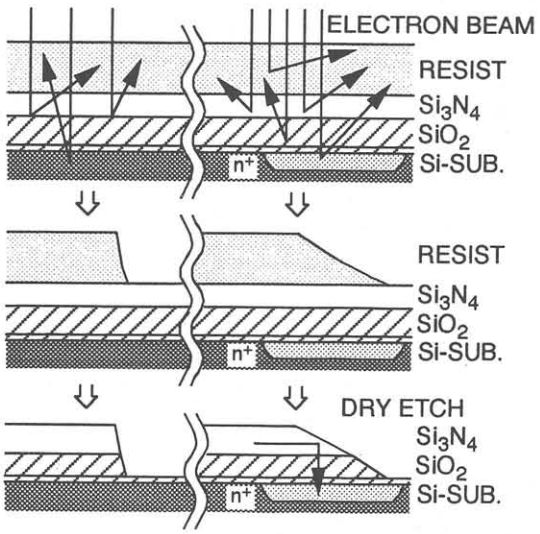

Fig. 5 Newly developed fabrication process for a micromirror.

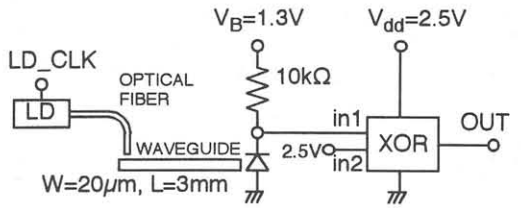

Fig. 6 Measurment circuit for testing a fabricated chip.

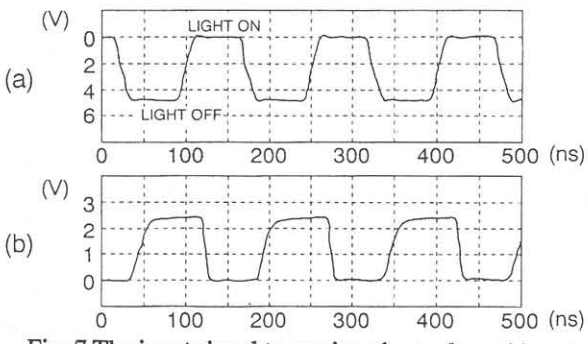

Fig. 7 The input signal to semiconductor laser (a) and the output signal from XOR circuit in Kohonen net (b).