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Stable Operation of Single Electron Logic Circuits with Feed-Back Loop

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Single electron devices based on Coulomb blockade phenomena in ultrasmall tunnel junctions are promising candidates of elemental devices in nm/angstrom-era's ULSI. Several kinds of SET (Single Electron Transistor) logic circuits have been proposed; resistance-loaded SET, capacitance-loaded SET, and complementary SET (CSET)[1] inverters. CSET seems to be the most promising as a primitive component of binary logic circuits, because the CSET inverter has a clear input-output characteristic, *i.e.*, $V_{out}=V_{DD}$ @$V_{in}=0$, $V_{out}=0$ @$V_{in}=V_{DD}$. However, design methodology of the conventional Si CMOS is not always applicable to CSET logic circuits. Novel CSET-NAND and NOR circuits which take account of the tunneling nature have been proposed and analyzed by Monte Carlo simulation.[2,3] Furthermore, when the operating temperature is increased, the stochastic tunneling affects the circuit operation, so that a new circuit configuration method is required for stable CSET logic operation.

In this paper, we propose and analyze the circuit operation of a new CSET circuits with a feed-back loop; a transfer-gate/flip-flop (FF) inverter as a primitive circuit component of SET logic circuits.

Circuit operation is analyzed by Monte Carlo simulation. In the simulator, circuit node equations are solved numerically, taking account of the charge re-configuration due to electron tunneling by the same manner reported by Osaka Univ's group.[2] Using the simulator, time dependent circuit operation can be analyzed for arbitrary SET circuits including the normal and tunnel capacitors and voltage sources.

Figure 1 shows the conventional CSET transfer-gate/inverter circuit. When the clock signal ϕ is logic "1" ($=V_{DD}$), the input voltage (V_{in}) is transferred to the inverter. Figure 2 shows switching characteristics with the output capacitance (C_{out}) of 360aF, in which fifteen electrons makes full logic swing. The relatively high operation temperature of 3.0K is assumed. The output voltage V_{out} varies according to V_{in} and ϕ. However, it is noted that the node voltage V_N does not keep a constant voltage as indicated by arrow-*A* in Fig. 2. This is due to the stochastic electron tunneling in transfer gates. When the time interval T_i becomes longer, V_N exceeds the inverter threshold of $0.5V_{DD}$ and V_{out} goes to "0" as shown in Fig. 3 (arrows-*B* and *C*). The transfer-gate/inverter circuit which is a primitive in logic circuits can not be operated any longer.

Figure 4 shows a new CSET logic circuit with a feedback loop; CSET transfer-gate/flip-flop (FF) inverter. The configuration is the same as Si CMOS FF circuit. When the voltage (V_N) varies due to the stochastic tunneling in the transfer gate, the output voltage (V_{out}) is expected to maintain a constant value because of a loop gain of the feedback loop. Figure 5 shows transit waveforms. It is confirmed that V_{out} varies according to V_{in} and ϕ, and V_N and V_{out} maintains a constant voltage of V_{DD}. In the above calculation, C_{out} is 360aF. When C_{out} is 12~24aF in which one electron makes full logic swing, the transfer- gate/FF-inverter is confirmed to have more stable characteristics than the conventional circuit of Fig. 1 with C_{out} = 24aF. The transfer-gate/FF-inverter has a potential use in CSET logic circuits, especially as a buffer circuit.

In summary, we have proposed a novel primitive logic circuit; "transfer-gate/flip-flop inverter". Monte Carlo simulation has shown that the novel circuit has more stable characteristics than the conventional CSET transfer/inverter circuit, because the voltage change due to the stochastic tunneling is compensated by the loop gain of the flip-flop circuits.

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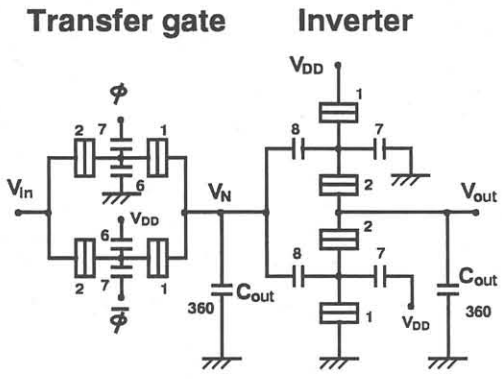

Fig.1 The conventional CSET transfer-gate/inverter.

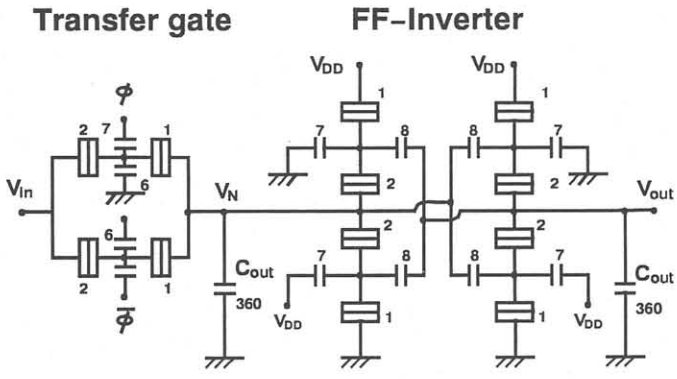

Fig.4 The new CSET transfer-gate/FF-type inverter.

The numerals are the value of each capacitor in unit of aF. The supply voltage (V_D) is 6.67mV = e/24aF. The tunnel resistance of tunnel capacitors is $5\times10^5\Omega$.

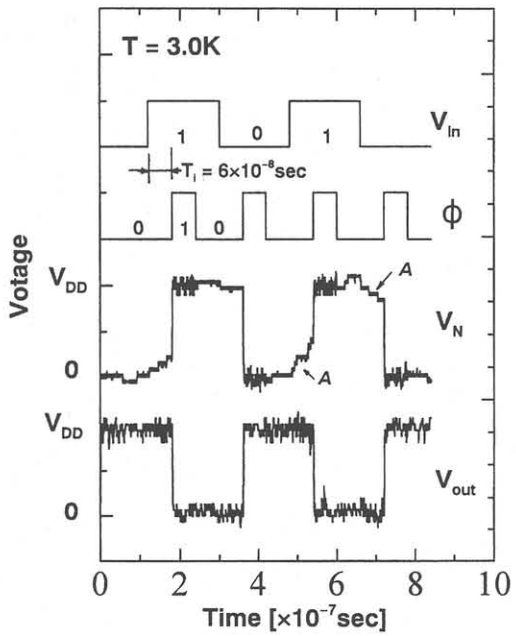

Fig. 2 Transit waveform of Fig. 1.

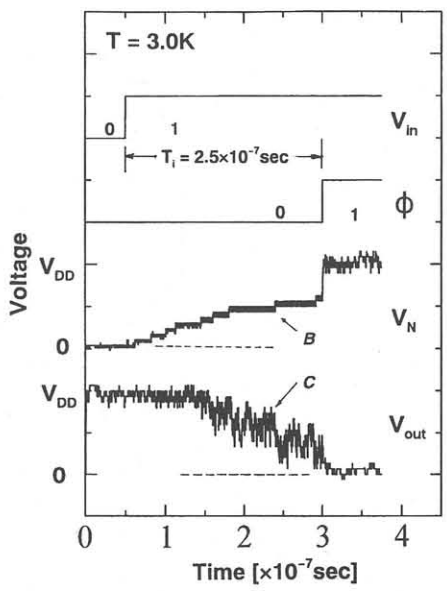

Fig. 3 Transit waveform of Fig.1. Clock cycle (T_i) is longer than that in Fig. 2.

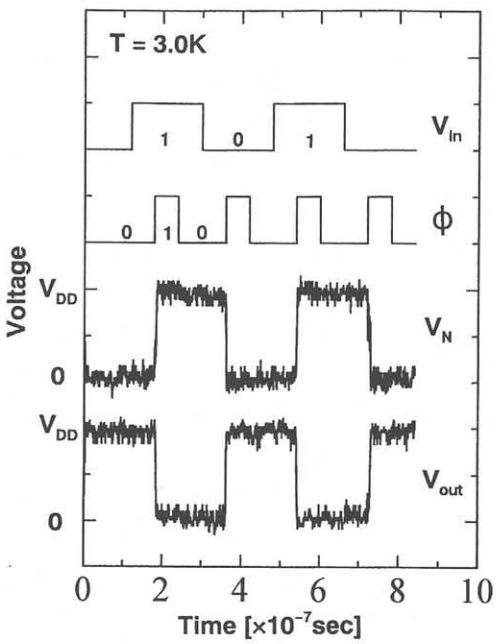

Fig. 5 Transit waveform of Fig. 4.

References

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(2) K. Taniguchi, M. Kirihara, N. Kuwamura and C. Hamaguchi, 13th Symp. on Future Electron Dev., 1994, p.34.

(3) M. Kirihara, N. Kuwamura, K. Taniguchi and C. Hamaguchi, 1994 SSDM, p. 328.