

## N<sub>2</sub>O-Anneal Induced Local Thinning of Regrown Oxide due to Nitrogen Residue at LOCOS Isolation Edges

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### Abstract

Effects of residual nitrogen at LOCOS isolation edges, remaining after stripping off oxynitrides (N<sub>2</sub>O-nitrided oxides), on the quality of the regrown gate oxides are studied. Current enhancement yielding the degradation was attributed to the local oxide thinning at the isolation edges. A quantitative model was also proposed to evaluate the leakage current of gate oxide at the LOCOS edges. Both electric characterization and photo emission study confirm the proposed model.

### I. Introduction

The demand on the quality and integrity of tunnel dielectrics in deep submicron flash EEPROM's has been increasingly stringent. Recently, lightly N<sub>2</sub>O oxynitride prepared by nitridation of SiO<sub>2</sub> in N<sub>2</sub>O ambient has received significant attention. Extensive researches [1-3] have been reported that N<sub>2</sub>O annealed gate oxides can improve the electrical stability of flash EEPROM's devices, such as excellent hot-carrier immunity, superior high field endurance. Slightly nitrogen incorporation at the oxide/substrate interface (about 1~3 atomic%) was speculated as the main cause of their excellent integrity and reliability. However, degradation effects due to residual surface nitrogen, remaining after stripping off oxynitrides on the integrity of regrown gate oxide were reported by Kim et al.[4]. In this work, local thinning of regrown gate oxide at LOCOS isolation edges caused by nitrogen residue was investigated by both electric characterization and photo emission study. A quantitative model was also proposed to evaluate the thinning of gate oxide at the LOCOS edges.

### II. Samples Preparation

Standard polysilicon gate MOS capacitors were fabricated. After 6500-Å field oxide formation by conventional LOCOS process, standard sacrificial oxidation and RCA cleaning was carried out before gate oxidation. Two categories of about 90-Å tunneling oxides were grown. One was grown in pure O<sub>2</sub> ambient. The other had initial oxide grown in pure O<sub>2</sub> followed by oxidation in N<sub>2</sub>O to the target thickness. Nitrogen concentration at the Si/SiO<sub>2</sub> interface, as measured by SIMS, was ~1%. A dilute HF solution was then used to strip off the first layer oxide. 160Å "OO" and "NO" gate oxides are regrown at the 875°C pure oxygen ambient on the silicon surface where a pregrowth pure and N<sub>2</sub>O annealed oxides were stripped off, respectively. Finally, standard n<sup>+</sup>-polysilicon gate technology with POCl<sub>3</sub> doping was used to fabricate MOS capacitors. Two

categories of test capacitors are used. One structure has field oxide edges under the n<sup>+</sup> poly gate which was called "field edge capacitor". The other structure without field oxide edges under the gate was called "gate edge capacitor". The schematic crosssection of test structures were illustrated in Fig. 1.

### III. Results and Discussion

Fig. 2 shows the current density(*J*) versus oxide field (*E<sub>ox</sub>*) curves for "NO" oxide under negative and positive gate biases. The gate current was measured under light illumination for a positive bias. For both negative and positive biases, the field edge structure shows a larger gate current than the gate edge structure, indicating an increase of the current at the isolation edges. Fig. 3 are the *J* versus *E<sub>ox</sub>* curves for "OO" oxide. No significant increase current observed in the field edge structure identified the increase current is caused by N<sub>2</sub>O annealed process. Local thinning of gate oxide[5] and/or locally intensified electric field by the buildup of positive charges[6] have been ascribed to the main cause of the current increment. Since the leakage current increment doesn't show significant bias polarity dependence, it is not reasonable to regard the positive charges only as the cause of leakage current increase. Residual nitrogen at the Si/SiO<sub>2</sub> interface is well known to act as a barrier for oxidant diffusion, it is speculated that nitrogen accumulated at the LOCOS edge during N<sub>2</sub>O annealing can not be fully stripped off. Consequently, leads to local oxide thinning and shifted *J* vs *E<sub>ox</sub>* characteristics.

To account for gate oxide thinning effect, a simple quantitative model was proposed and illustrated in Fig. 4. *I<sub>ga</sub>* denotes the Fowler-Nordheim electron tunneling in the capacitor area. *I<sub>gp</sub>* represents the electron tunneling in the field oxide edge region. The formula of Fowler-Nordheim tunneling current is written below,[7]

$$I = A_{cap} A_{fn} F^2 \exp(-B_{fn}/F) \quad (1)$$

*A<sub>cap</sub>* represents the tunneling area. Fig. 5 compares the calculated *I<sub>ga</sub>* and measured gate currents for gate edge structure under negative gate biases. A good fit is obtained with *A<sub>fn</sub>* = 3.0 × 10<sup>-6</sup> Amp/V<sup>2</sup> and *B<sub>fn</sub>* = 251 MV/cm. These values are comparable with those cited in the literature[8]. In this work, the gate oxide quality at the field oxide edge was assumed to be the same as that in the capacitor area. Thus, only a set of physical constant *A<sub>fn</sub>* and *B<sub>fn</sub>* was used. Fig. 5 shows the validation of the proposed model by a comparison between calculated *I<sub>ga</sub>* + *I<sub>gp</sub>* and measured gate leakage current for field edge capacitor. A 500-Å thinning area with 115-Å oxide thickness unless of target 160-Å oxide thickness was

found to best fit the measured gate current. The oxide breakdown voltage under negative gate biases, defined as the voltage at which the gate current reach to  $-10\text{mA}$ , was also studied. Fig. 6 plots the breakdown voltage in the gate edge structure as a function of oxide thickness. The breakdown voltage of field edge structure was also shown in Fig. 6 for comparison. The field edge structure shows a similar breakdown voltage to that of the gate edge structure with  $115\text{-}\text{\AA}$  oxide. Such a breakdown result is consistent with our quantitative F-N thinning model.

The gate leakage currents for both structures are further characterized in  $1.0\text{E-}4\text{ cm}^2$ ,  $1.6\text{E-}3\text{ cm}^2$ , and  $1.0\text{E-}2\text{ cm}^2$  capacitors. A roughly constant leakage current density in the gate edge capacitors especially for the small area samples in Fig. 7 indicate that the  $\text{N}_2\text{O}$  annealing process has no significant influence on the regrown oxide quality in the active regions without field oxide edges. Figure 8 shows the relationship between the perimeter length and leakage current in the field edge capacitors. The increase gate current with increasing perimeter length confirms the leakage current enhancement at the isolation edges.

Fig. 9 shows the photo emission result from the field edge capacitor under a oxide breakdown condition. The light spot observed near the LOCOS edges confirms the effects of local oxide thinning at the edges due to residual nitrogen.

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#### References

- [1] Y. S. Kim *et al.*, "Low-Defect-Density and High-reliability FETMOS EEPROM's fabricated using furnace  $\text{N}_2\text{O}$  oxynitridation", *IEEE Electron Device Lett.*, vol. 14, no. 7, p. 342, 1993
- [2] H. Fukuda, M. Yasuda, T. Iwabuchi, and S. Chno, "novel  $\text{N}_2\text{O}$ -oxynitridation technology for forming highly reliable EEPROM tunnel oxide films," *IEEE Electron Device Lett.*, vol. 12, no. 11, p. 587, 1991.
- [3] U. Sharma *et al.*, "Vertically scaled, high reliability EEPROM devices with ultra-thin oxynitride films prepared by RTP in  $\text{N}_2\text{O}/\text{O}_2$ ," in *IEDM Tech. Dig.*, 1992, p.461.
- [4] J. Kim, A. B. Joshi, G. W. Yoon, and D. L. Kwong, "Effects of residual surface nitrogen on the dielectric breakdown characteristics of regrown oxides," *Proc. of Symp. on VLSI-TSA*, p.100, 1993
- [5] A. Bhattacharyya, C. Vorst, and A. H. Carim, "A two-step oxidation process to improve the electrical breakdown properties of thin oxides," *J. Electrochem. Soc.*, vol. 132, no. 8, p.1900, 1985

- [6] I. C. Chen, S. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vol. ED-32, p. 413, 1985.
- [7] M. Lenzlinger and E. H. Snow, Flower-Nordheim into thermally grown  $\text{SiO}_2$ ," *J. Appl. Phys.* vol. 40, pp.278-283,1969
- [8] Z. A. Weinberg, On tunneling in metal-oxide silicon structures," *J. Appl. Phys.*, vol. 53, pp.5052-5056, 1982

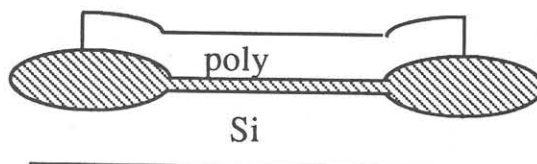


Fig. 1(a) Field edge capacitor

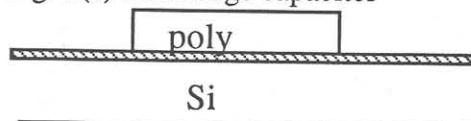


Fig. 1(b) Gate edge capacitor

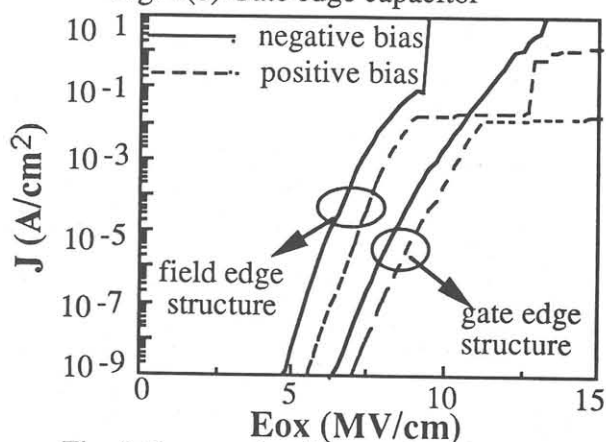


Fig. 2 Current density vs. electric field for "NO" oxide.

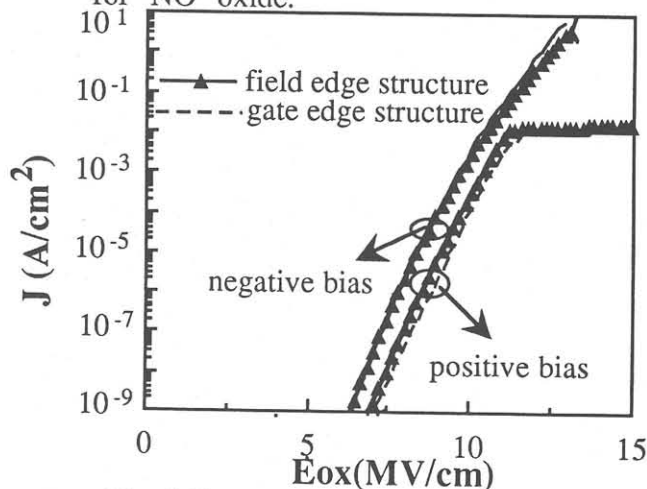


Fig. 3 Current density vs. electric field for "OO" oxide.

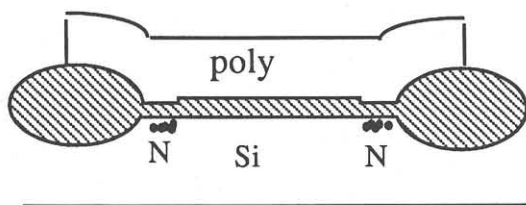


Fig.4 A conceptual diagram of the present model.

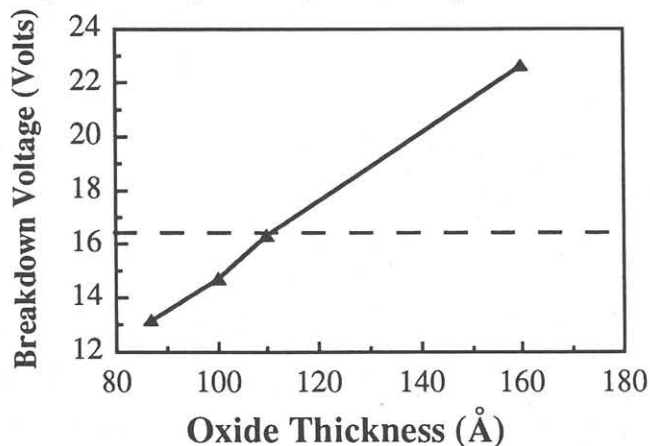


Fig. 6 Breakdown voltages in gate edge structure. as a function of oxide thickness . Dash line is the breakdown voltage of field edge structure with 160Å gate oxide

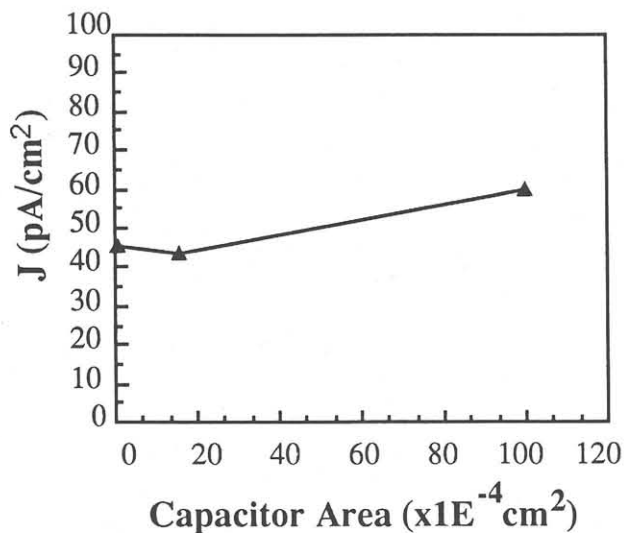


Fig. 7 Relationship between leakage current density to capacitor area for gate edge structure.

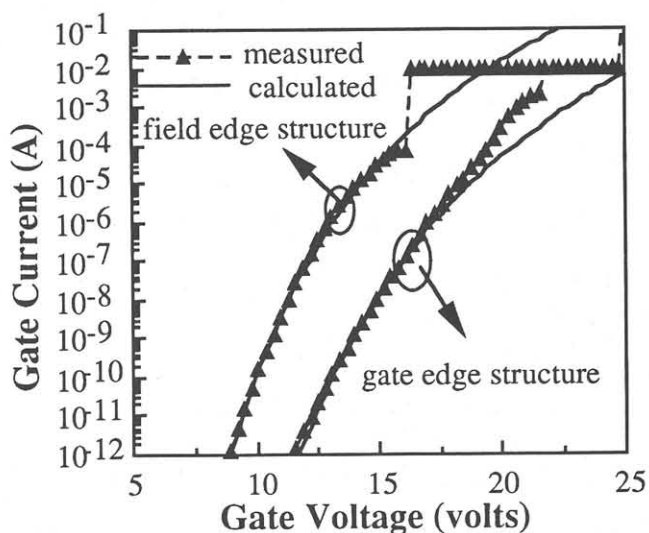


Fig. 5 The calculated gate current as a function of gate voltage. The associated experimental data are deduced from Fig. 2 for comparison.

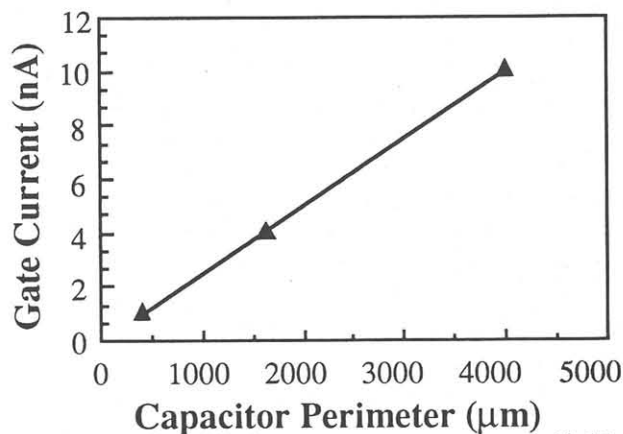


Fig. 8 Relationship between gate current to field edge capacitor Perimeter .

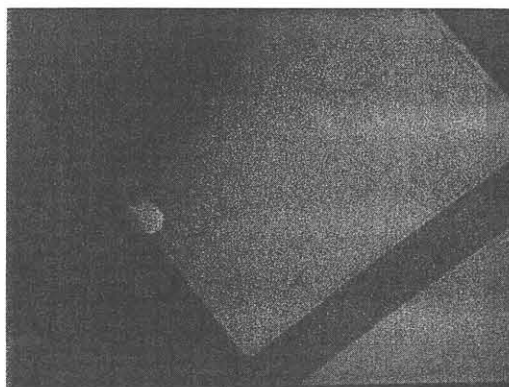


Fig. 9 An example of photon emission from field edge structure under breakdown condition.