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Excellent Quality of SiO_2 Dielectric Film Prepared by Room-Temperature Ion Plating and Its Application to Thin-Film Transistors

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The physical and electrical properties of SiO_2 film deposited by ion plating at room temperature reveal that the film is a high-density dielectric with strained bonds. The characteristics in total show that the film is a high-performance dielectric for low temperature applications.

1. INTRODUCTION

Low-temperature deposited dielectric films with excellent electronic qualities are required for microelectronics and thin-film transistors (TFTs) technology. The conventional PVD or CVD methods for depositing SiO_2 films exhibit the problems of porosity or high impurity content[1), 2)]. To prepare high performance SiO_2 films at low temperature, the ion plating (IP) method was developed. The IP oxides have been successfully used for optical applications, and show dense microstructures, smooth surfaces, and stoichiometry[3)]. In this work, we investigated the characteristics with ellipsometry, FTIR, P-etch solution, and electrical measurements. The annealing effects on IP SiO_2 were also investigated. Finally, we also apply the oxide as gate insulator to TFTs.

2. EXPERIMENTAL

The low-voltage reactive IP SiO_2 film was prepared in Balzers BAP 800 system[3)]. The staring material, silicon was evaporated by electron beam evaporator. The 3.9 mbar argon in plasma source cavity was ionized by the heated filament. The oxygen gas was let directly into the deposition chamber. The partial Ar pressure in the deposition chamber is 3×10^{-4} mbar during deposition. The total chamber pressure was fixed at 1.1×10^{-3} mbar, while the base pressure was 4.4×10^{-5} mbar. The substrate obtained a negative self-bias of -10 to -20 V from the plasma sheath. Oxide films were deposited at room temperature with deposition rate of 0.2 nm/s.

The 97.6 nm IP SiO_2 was deposited on p-type Si(100) substrates. Annealing treatments were performed in N_2 for 30 min at 400°C, 600°C, and 800°C, respectively. To investigate the electrical properties of the oxide, MOS capacitors with Al gate were prepared. The comparison with thermal oxide (~97 nm) grown at 1000°C in dry O_2 was also studied.

The n-channel poly-Si TFTs with 50 nm-IP SiO_2 as gate insulator were frabricated. The 100 nm-thick active layer was prepared by SPC method. Hydrogenation was performed at 300°C for 60 min.

3. RESULTS and DISCUSSION

A. Physicochemical Properties of IP SiO_2 Films

Figure 1 shows the changes of FTIR Si-O-Si stretching frequency (ν) and FWHM under different annealing temperatures. The lower stretching frequency (1056 cm^{-1}) and the broader FWHM (87.4 cm^{-1}) of as-deposited SiO_2 indicate that there are strained bonds existed in the room temperature deposited IP SiO_2 films[2)]. As the annealing temperature increases, the stretching bonds shift to higher frequency and FWHM becomes narrower. It implies that the strained bonds are relieved after high temperature annealing.

In the context of force constant models for the vibrational properties[4), 5)], the frequency of Si-O bond stretching vibration was given by $\nu = \nu_0 \sin(\theta/2)$, where ν_0 is 1117 cm^{-1} [6)] and θ is the Si-O-Si bond angle. The Si-Si distance ($d_{Si\text{-}Si}$) is directly related to the Si-O-Si bond angle by the relationship $d_{Si\text{-}Si} = 2r\sin(\theta/2)$, where r is Si-O bond length (1.504 Å)[7)]. Table I shows the changes of ν, θ, and $d_{Si\text{-}Si}$ with annealing temperatures. After high temperature annealing, θ and $d_{Si\text{-}Si}$ increase. These increases also imply that the strained bonds have been relieved and tend to the thermal Si-O-Si network.

To determine the density (ρ) of IP SiO_2, we measure refractive index (n) by ellipsometer. The relationship between n and ρ can be described as $\rho = K\cdot(n^2-1)/(n^2+2)$, where K is 8.046[7)]. Figure 2 shows n and ρ decrease as the films were annealed at high temperature. For as-deposited IP SiO_2, ρ is 2.298 g/cm^3 obtained from n of 1.483. Therefore, the IP SiO_2 is a high density material without porosity, which is the characteristic of the ion plating method[8)]. After 800°C annealing, n and ρ decrease, and tend toward those of thermal SiO_2. It is consistent with the relief of strained bonds after high temperature annealing.

Figure 3 shows that the P-etch rate decreases with annealing temperature. The P-etch rate of as-deposited films is 4.9 Å/s. Compared to 2 Å/s of thermal SiO_2, the higher etch rate is caused by strained bonds[2]. The decrease in etch rate after annealing is also due to the relief in strained bonds.

B. Electrical Properties of IP SiO_2 Films

Figure 4 shows the quasi and high-frequency C-V curves of IP SiO_2 MOS capacitors. The interface state density is 1.8×10^{10} eV^{-1} cm^{-2}. The flat-band voltage (V_{fb}) of -0.675 V means that an excess of negative charges exists in the oxide. No hysteresis effect is observed, and V_{fb} is also independent of bias conditions. Figure 5 shows the changes of V_{fb} and effective oxide charge N_{eff} with annealing temperature. The V_{fb} and negative charges decrease after annealing.

The J-E characteristics of MOS capacitors after annealing are shown in Fig. 6. The leakage density of IP SiO_2 is about 10^{-9} A/cm^2 at the electric field of 4 MV/cm and comparable with that of thermal SiO_2. The breakdown electric field is over 9 MV/cm. For the as-deposited and the 400°C annealed samples, the slope of J-E curves at high electric field region (>8 MV/cm) decrease. This is because these samples trap more electrons at this region, and their strained bonds can be easily broken by injecting electrons[9), 10]. As annealed more than 600°C, the strained bonds are relieved. The leakage current becomes the typical Fowler-Nordheim tunneling current without reduction at high electric field region.

Figure 7 shows Fowler-Nordheim plots of tunneling data from Al into SiO_2. The barrier height between Al electrode and the as-deposited IP SiO_2 is 2.71 eV. Compared to thermal oxide (~ 3.01 eV), the lower barrier height is caused by some traps existed in the oxide film [10].

In total, the qualities of IP SiO_2 are rather satisfactory, and indicate the film to be a good candidate as the gate dielectric in low-temperature processed (LTP) devices.

C. Performance of LTP Poly-Si TFTs

Figure 8 shows the I_{DS}-V_{GS} transfer characteristics of as-fabricated and hydrogenated poly-Si TFTs at V_{DS} = 5V (W/L = 20 μm/5 μm). The ON/OFF current ratio (I_{ON}/I_{OFF}) is 4×10^6 after hydrogenation. The field-effect mobility (μ) of 16.1 $cm^2/V \cdot s$ at V_{DS} = 0.1V, the threshold voltage (V_{th}) of 7.13 V, and the subthreshold swing (S.S.) of 1.47 V/dec are obtained. The excellent characteristics of poly-Si TFTs show the feasibility of IP SiO_2 as the gate dielectric in LTP poly-Si TFTs.

4. CONCLUSION

Room-temperature deposited ion plating SiO_2 has dense microstructure and strained bonds. After high temperature annealing, density and strained bonds decrease. The breakdown field of the MOS capacitor is over 9 MV/cm. The characteristics are comparable with that of thermal SiO_2. The excellent poly-Si TFT with IP SiO_2 as gate insulator has been fabricated successfully. The quality of the ion plating oxide is satisfactory for the requirement of gate dielectrics in low-temperature processed devices.

Acknowledgment

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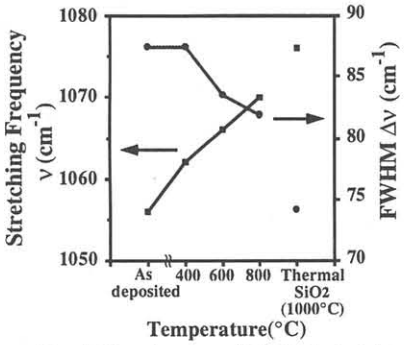

Fig. 1 The changes of Si-O-Si stretching frequency (ν) and FWHM (Δν) with annealing temperature.

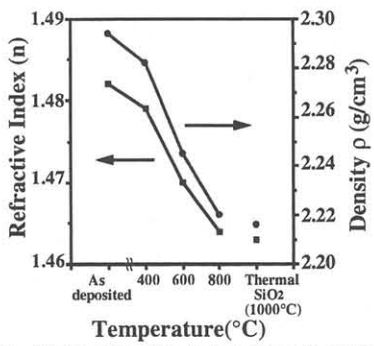

Fig. 2 The refractive index (n) and density (ρ) of IP SiO2 decrease with annealing temperature.

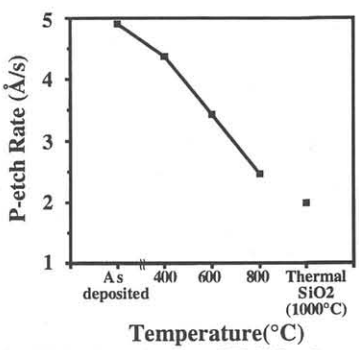

Fig. 3 The P-etch rate of IP SiO2 decreases with annealing temperature.

Table I The changes of Si-O-Si stretching frequency, bond angle and Si-Si distance with annealing temperature.

Anneal Temperature (°C)	Si-O-Si Stretching Frequency ν (cm^{-1})	Si-O-Si Bond Angle (θ°)	d_{Si-Si} (Å)
as-deposited	1056	141.95	2.844
400	1062	143.89	2.860
600	1066	145.24	2.871
800	1070	146.64	2.881
Thermal SiO_2	1076	148.86	2.898

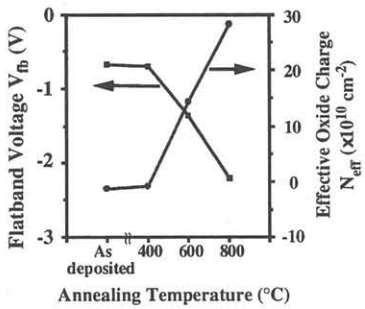

Fig. 5 The changes of flat-band voltage and effective oxide charge in IP SiO2 MOS capacitor with different annealing temperature.

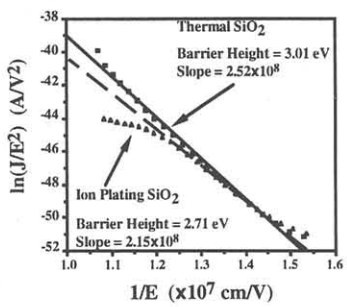

Fig. 7 Fowler-Nordheim plots of tunneling data from aluminum into SiO2.

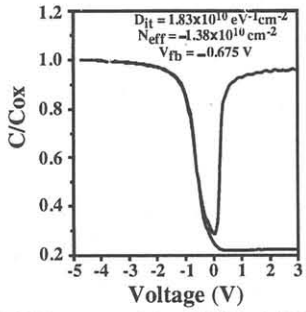

Fig. 4 C-V curves of the IP SiO2 MOS capacitor.

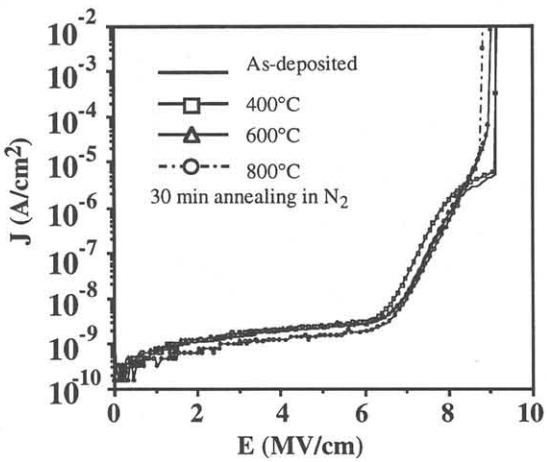

Fig. 6 J-E characteristics of IP SiO2 after different high-temperature annealing.

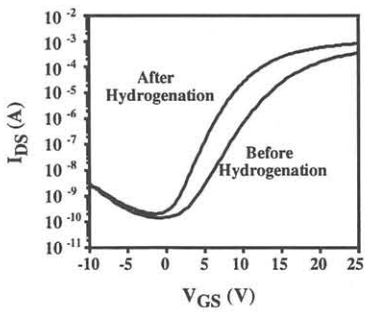

Fig. 8 Transfer characteristics of LTP poly-Si TFTs at V_{DS} = 5V before and after hydrogenation.