Characterization of One-Dimensional Conduction in an Ultra-Thin Poly-Si Wire

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One-dimensional conduction in ultra-thin poly-Si single-electron devices is studied. A model, which includes a transition from one-dimensional conduction to two-dimensional conduction as gate voltage is increased, explains experimental results well. Unprecedented 60% modulation of current by random telegraph noise at room temperature has also been observed.

1. Introduction

Single electron devices, in which an addition or subtraction of an electron can be controlled by using a charging effect, have recently attracted much attention [1]. We have succeeded in room temperature operation of single electron memories and transistors by introducing ultra-thin (~3-nm) poly-Si film in which natural one-dimensional current path beyond lithography limit less than 10-nm is achieved [1, 2]. We believe that an ultra-thin poly-Si film is one of the most promising platforms we have now to probe single-electron effects. In the previous works, however, study of the conduction in the films was limited to low electron density region because the gate oxide thickness was so large that the electron-density cannot widely be changed. In this work, using new samples having thinner gate oxide we characterize the conduction in this ultra-thin poly-Si wire in wide electron-density range. Especially, we study a transition from one-dimensional conduction under near threshold voltage condition to two-dimensional conduction under higher gate voltage condition.

2. Device Structure

The fabricated device consists of an ultra-thin channel poly-silicon wire (3-nm thick) and a gate wire (80-nm thick) which covers the channel wire. Thickness of the gate oxide is 30-nm. The channel poly-silicon film is deposited as a-Si and crystallized at 750°C and consists of silicon grains, each about 10-nm across (Fig. 1).

In our picture, current path width under low current condition is comparable to the typical grain-size of the poly-Si film, and the width spreads as gate voltage is increased. Because there is thickness variation in the poly-Si film, the potential in the film, which originates mainly from vertical quantum confinement energy, varies randomly depending on the position. As we apply a positive gate bias, low-potential regions below the Fermi level are filled with electrons, and finally a percolation channel between source and drain is formed (Fig. 1). Then the current bottleneck of the channel is much narrower than physical wire width. The current-path width is expected to spread as gate voltage soars, because regions below the Fermi level increase.

3. Variable Channel-width Model

To take this width change effect into account, following simple model is formulated. We assume that a poly-Si wire consists of many fine wires that have different threshold voltages, which are scattered uniformly between V_{min} and V_{max} (Fig. 2). Here V_{min} is the lowest threshold voltage of fine wires in the film and V_{max} is the highest threshold voltage. Then, in this model effective current-path width W_{on} is given by following equation.

$$W_{on} = (V_G - V_{min}) W / \Delta$$

where V_G is the gate voltage and Δ is ($V_{max} - V_{min}$). Applying gradual channel approximation to each fine wire and integrating, we get equations shown in Table 1, which are compared with the conventional fixed channel width model. In saturation region, current-voltage characteristics are proportional to $(V_G-V_{th})^3$ in this model, which is different from $(V_G-V_{th})^2$ in conventional model. And in linear region, current depends on $(V_G-V_{th})^2$, which is higher power of (V_G-V_{th}) than linear dependence of conventional model. Under enough high gate voltage condition, which is higher than V_{max}, current depends on (V_G-V_{th}) linearly because the current-path width corresponds to physical wire width and this model gives same results with conventional model in this region.

4. I-V Characteristics

Experimentally, the current-voltage characteristics of our devices show different behaviour from usual FET's characteristics. Channel width of sample changes from 0.07-μm to 2-μm. Each sample has same channel length, which is 0.2-μm. I-V characteristics are shown in Fig. 3 and Fig. 4. Although the current increases exponentially as gate voltage is increased in subthreshold region just like usual FET (Fig. 3), in saturation region, the current-voltage characteristics are not proportional to $(V_G-V_{th})^2$ but are proportional to $(V_G-V_{th})^3$. And in linear region, the current depends on higher power of (V_G-V_{th}) than linear dependence. It is clear that our model describes much better the I-V curve of our devices than conventional model.

Using variable channel-width model, we can estimate current-path width from experimental I-V characteristics as following procedure. From equations shown in Fig. 1, second derivatives in saturation region and first derivatives in linear region are proportional to current width W_{on} respectively. Then from the ratio between these two quantities, we can get the ratio between W_{on} under high-voltage condition and W_{on} under low-current condition if the mobilities under two conditions are not that different. Based on our model in which W_{on} spreads proportionally to W as gate voltage increases, this ratio is proportional to W. On the other hand, this ratio is independent of W in fixed channel approximation. Evaluated ratios between W_{on} at the high gate voltage and W_{on} under the low gate voltage depend linearly on W, which agrees well with what our model predicts (Fig. 5). Assuming that the current-path width W_{on} at $V_G=7V$ is close to W, we get current-path width near threshold about 10-nm, which is comparable to the typical lateral grain-size of the poly-Si film. Therefore, quasi-one-dimensional current path is formed in our ultra-thin poly-Si device under low current condition.

5. Random Telegraph Noise

One feature of one-dimensional conduction appears in large random telegraph noise. Time dependence of the drain current under fixed gate voltage and drain voltage at room temperature is shown in Fig. 6. Transitions between two states, which correspond to single electron capture and release, are clearly observed. This random telegraph noise with over 60 % current modulation is unprecedented large. In a one-dimensional path, repulsive Coulomb force works effectively and only one electron trap significantly affects the current. From this current modulation and I-V curve of this device, we can estimate capacitance between the gate and the bottleneck region in the current-path. And from this capacitance value, which is about 0.4-aF, the current-path width is estimated to less than 20-nm.

6. Conclusions

We have demonstrated that our model taking into account of gate-voltage dependence of current-path width explains experimental I-V characteristics of the single electron devices which use an ultra-thin poly-Si film well. Using this model, we show the current-path width of the device under the low current condition is about 10-nm, which is comparable to the typical lateral grain-size of the film. We also observed unprecedented large random telegraph noise at room temperature. This is a feature of one-dimensional conduction. These results support our picture for the device operational principles of our single electron memory and transistor.

References

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[3] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, Int. Conf. on Solid State Devices and Materials, p325 (1994)
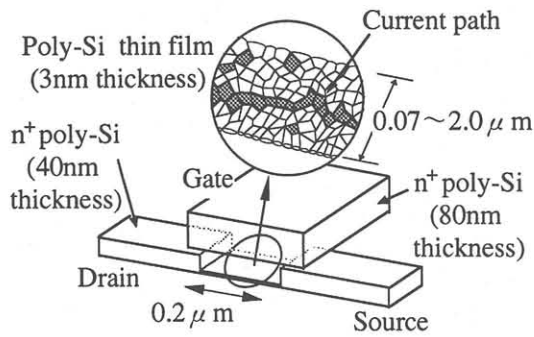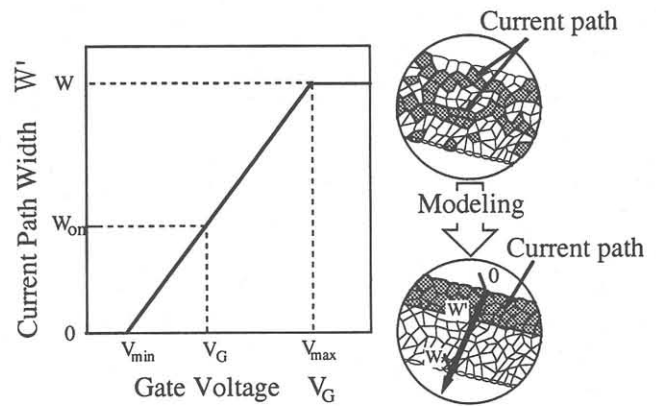
Poly-Si thin film (3nm thickness)
n⁺ poly-Si (40nm thickness)
Gate
Current path
$0.07 \sim 2.0\,\mu m$
n⁺ poly-Si (80nm thickness)
Drain
$0.2\,\mu m$
Source

Fig1　Fabricated structure

Current path
Modeling
Current path

Fig. 2　Gate-current path-width relation in the model
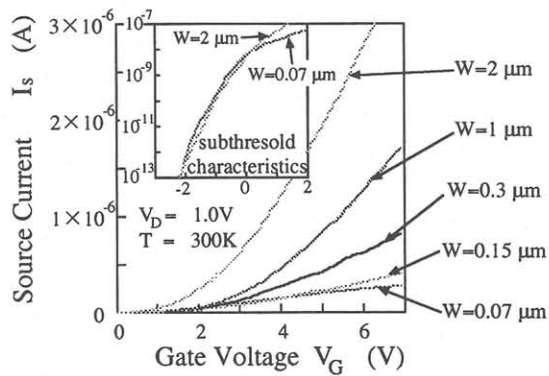
Fig. 3　Current-voltage characteristics

$I_S \propto (V_G - V_{th})^2$
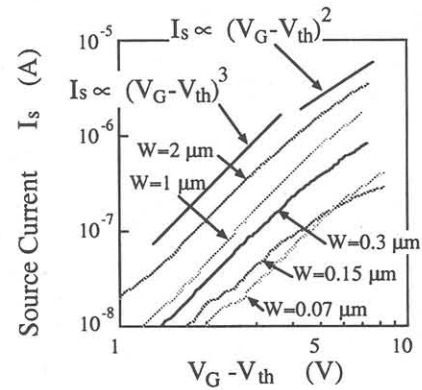$I_S \propto (V_G - V_{th})^3$
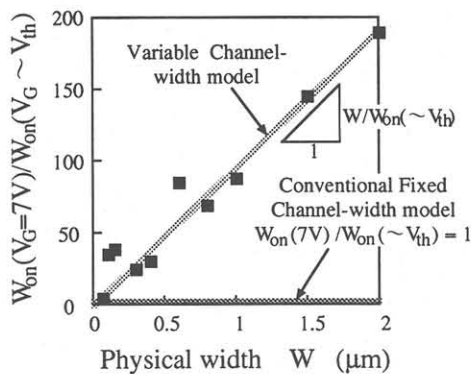
Fig. 4　Current dependence of gate voltage

Fig.5　Current-path width ratio between low current condition and high voltage

Fig.6　Source current fluctuation
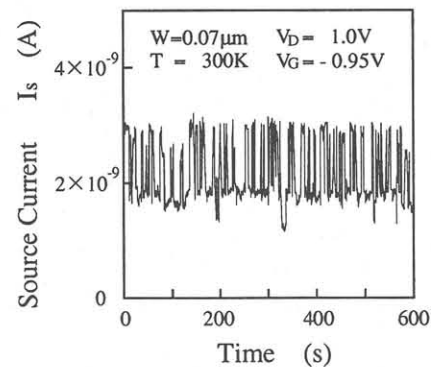
Table. 1　Variables of I-V characteristics

	saturation region $(V_G < V_D + V_{th})$	linear region $(V_G > V_D + V_{th})$
Variable Channel-width model	$I_D = \dfrac{\beta}{6\Delta}(V_G - V_{min})^3$ $\downarrow$ $\dfrac{d^2 I_D}{dV_G^2} = W_{on}\mu C_{ox}/L$	$I_D = \dfrac{\beta V_D}{2\Delta}(V_G - V_{min})^2$ $\downarrow$ $\dfrac{1}{V_D}\dfrac{dI_D}{dV_G} = W_{on}\mu C_{ox}/L$
Conventional Fixed Channel-width model	$I_D = \dfrac{\beta}{2}(V_G - V_{th})^2$ $\downarrow$ $\dfrac{d^2 I_D}{dV_G^2} = W\mu C_{ox}/L$	$I_D = \beta\{(V_G - V_{th})V_D - \frac{1}{2}V_D^2\}$ $\downarrow$ $\dfrac{1}{V_D}\dfrac{dI_D}{dV_G} = W\mu C_{ox}/L$

$\beta = W\mu C_{ox}/L$, $\Delta = V_{max} - V_{min}$