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Complementary Digital Logic Using Resistively Coupled Single Electron Transistor

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A new complementary digital logic based on resistively coupled single-electron-transistors (R-SET) was proposed and its basic characteristics were numerically analyzed using the Monte Carlo method. The proposed logic has a logic threshold independent on back ground polarization charges which induce crucial problems in logic operation in the case of a capacitively coupled logic. In addition, the proposed complementary R-SET logic has lager output voltage swing and larger logic level stability than those of a conventional resistance load R-SET logic.

1. Introduction

Recently, single-electron digital logics[1,2] are attracting many researcher's attention because of their potential operation with very low power consumption and high circuit density. There have been proposed many types of SET devices up to date, such as capacitively coupled transistor, resistively coupled transistor, complementary logic circuit,[3] turnstile device, pump device, and multiple-tunnel junction memory *etc.*, and their basic characteristics have been verified experimentally.

Among these devises, a resistively coupled single-electron-transistors (R-SET) is thought to be one of the most important element in making large scale digital logic circuits, since it has large voltage gain and stability of a logic threshold against back ground polarization charges on isolated electrodes. The existence of the random polarization charges near each tunnel junctions makes it impossible to realize accurate logic operation of large scale integrated circuits using capacitively coupled SET (C-SET) gates. In spite of this advantage of the R-SET gates, it was pointed out that they have very small logic revel difference[4] due to their high on-state resistance compared to the C-SET gates. In this report, we will propose a new complementary digital logic based on the R-SET to overcome this disadvantage, and analyze numerically its basic characteristics using the Monte Carlo method.

2. Complementary Logic Using R-SET

Figure 1 (b) shows basic cell of the complementary R-SET inverter, where a load resistance of the conventional resistance load R-SET inverter (see Fig.1 (a)) is replaced by a pull-up R-SET. The bias capacitance, which must be connected to the center electrode of the SET in the complementary C-SET logic, is not necessary for the complementary R-SET logic.

In order to investigate switching operation of the complementary R-SET inverter, we divide it into two parts; namely, a pull-down switch and a pull-up switch as shown in Fig. 2 (a) and Fig. 3 (a), respectively. For the simplicity of consideration, it is assumed that the output resistance R_{out} and capacitance C_{out} are very large compared to the resistance $R_{1,2}$ and capacitance $C_{1,2}$ of the tunnel junction. In Fig. 2 (a), when the input voltage V_{in} is applied to the input node, the condition that the lower tunnel junction of the pull-down switch is in the Coulomb blockade state is represented as

$$|eV_{in}| < E_c, \tag{1}$$

where $E_c=e^2/(C_1+C_2)$ is a charging energy for the single electron tunneling. The condition that the upper tunnel junction is in the Coulomb blockade state is also given by

$$|e(V-V_{in})| < E_c. \tag{2}$$

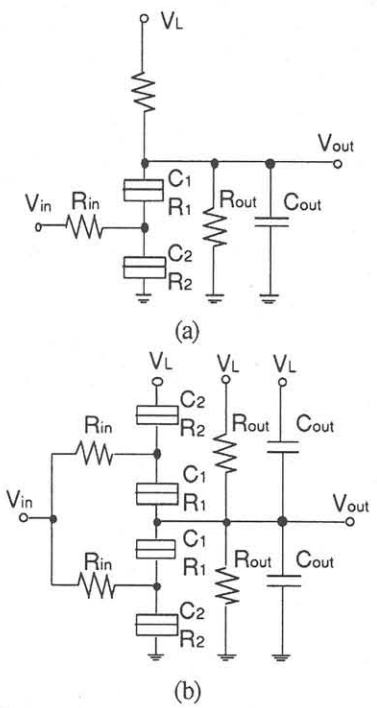

Fig. 1. (a) Conventional resistance load R-SET inverter. (b) Complementary R-SET inverter.

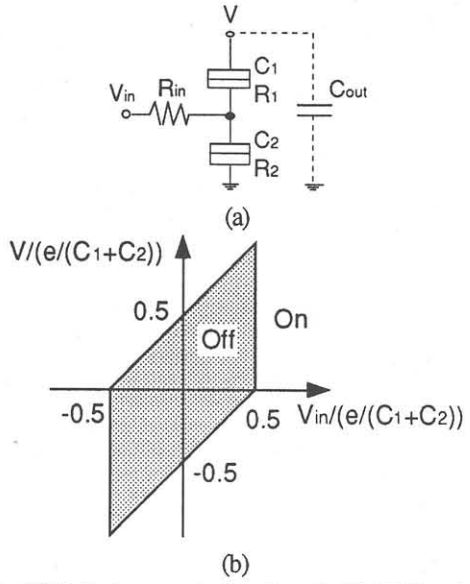

Fig. 2. (a) Pull-down switch using the R-SET and (b) its mode diagram. ($C_{out}>>C_{1,2}$ and $R_{out}>>R_{1,2}$).

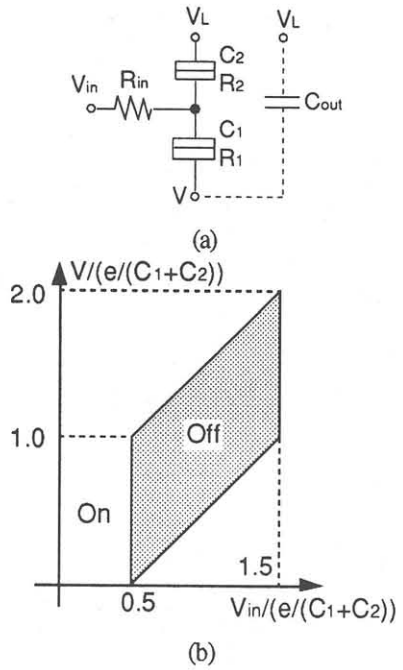

Fig. 3. (a) Pull-up switch using the R-SET and (b) its mode diagram when $V_L=e/(C_1+C_2)$. ($C_{out}>>C_{1,2}$ and $R_{out}>>R_{1,2}$).

These conditions are plotted in Fig. 2 (b) as a shaded area, in which both the tunnel junctions is in the Coulomb blockade state, resulting in the off-state of the pull-down switch. Outside this region, one of the tunnel junction is at least in the conducting state, and then the whole pull-down switch falls into the conducting state due to the space correlation of the single electron tunneling.

The behavior of the pull-up switch will be obtained from those of the pull-down switch by the following transformations

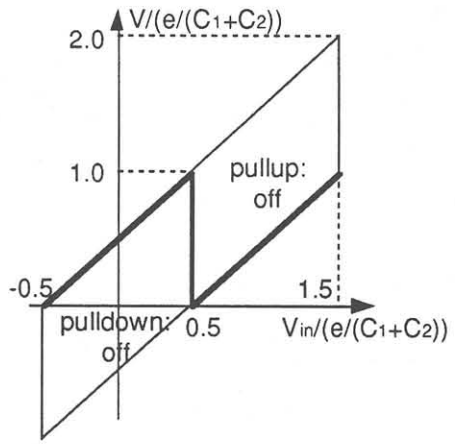

Fig. 4. Transfer characteristics of the complementary R-SET inverter in Fig. 1 (b) when $V_L=e/(C_1+C_2)$.

$$V\rightarrow(V_L-V),\quad V_{in}\rightarrow(V_L-V_{in}), \tag{3}$$

where V_L is a load voltage. In Fig. 3 (b) is shown the off-state region of the pull-up switch as a shaded area, when $V_L=e/(C_1+C_2)$.

The voltage transfer characteristics of the complementary R-SET inverter are derived directly by combining the mode diagram of the pull-down and pull-up switch as illustrated in Fig. 4. When an input voltage V_{in} is less than the threshold voltage $V_{th}=0.5\times e/(C_1+C_2)$, the pull-down switch is in the off-state and the pull-up switch in on-state, and vice versa. Then the output voltage V_{out} changes along the solid curve in Fig. 4 as the input voltage is varied. It is found from the figure that the voltage gain and the logic level difference of the complementary R-SET inverter are very large compared to the resistance load R-SET inverter.

3. Calculation Results and Discussion

All calculations in this study are based on the semi-classical model using the Monte Carlo method.[4,5] In calculations, we ignore the cotunneling process and the quantum fluctuation which otherwise must be considered when the resistance of the tunnel junction is not large compared to the critical resistance.

Figure 5 shows calculated voltage transfer characteristics of the complementary R-SET inverter for various values of the output resistance R_{out} at very low temperature. The calculated results are similar to the theoretical curve in Fig. 4 when R_{out} is very large, but the difference between them becomes obvious as R_{out} is decreased. Though the voltage gain and the logic level difference tend to be reduced with decrease of R_{out}, which is attributed to draining of the charge on the output capacitance C_{out} by R_{out} in high rate, the inverter is found to have enough ability to drive the next-stage inverter of the same type. The logic level difference is about twice as large as that of the conventional resistance load R-SET inverter.[4]

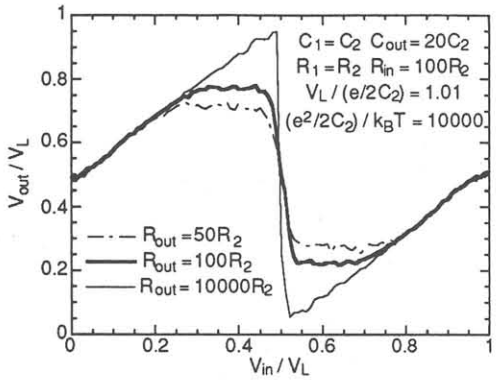

Fig. 5. The voltage transfer characteristics of the complementary R-SET inverter.

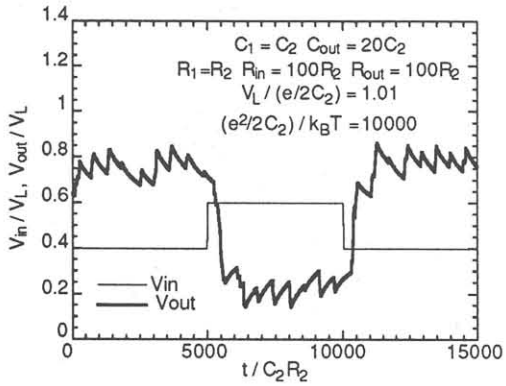

Fig. 6. Switching waveform of the output node voltages of the complementary R-SET inverter.

Switching waveform of the output node voltage of the complementary R-SET inverter is shown in Fig. 6, when a step function voltage is applied to the input node. It can be seen in the figure that the output waveform is an oscillating function of time in both a logic level "1" and a logic level "0" because of stochastic tunneling events of single electrons through the R-SET. By taking an ensemble average of the output waveform, we estimate a time constant in an upward and downward switching to be $\sim 530 R_2 C_2$ when using the circuit parameters in Fig. 6. This value is thought to be equal to the time constant $C_{out} \times (2R_{ON} // R_{out})$ which is determined by the output capacitance C_{out}, the on-state resistance of the R-SET R_{ON}, and the output resistance R_{out}. Using $C_{out}=20C_2$ and $R_{out}=100R_2$, we obtain $R_{ON} \approx 18R_2$, which is consistent with R_{ON} derived from the *I-V* characteristics.

In order to verify the stabilities of the logic level in a long chain of the inverter, we examined the characteristics of a cross-coupled latch circuit shown in Fig. 7 (a). Time average of the output node voltages V_{out1} and V_{out2} of the cross-coupled latch circuit as a function of an initial input node voltage V_{in0} is shown in Fig. 7 (b). One can clearly see that the logic levels remain stable even in the long chain.

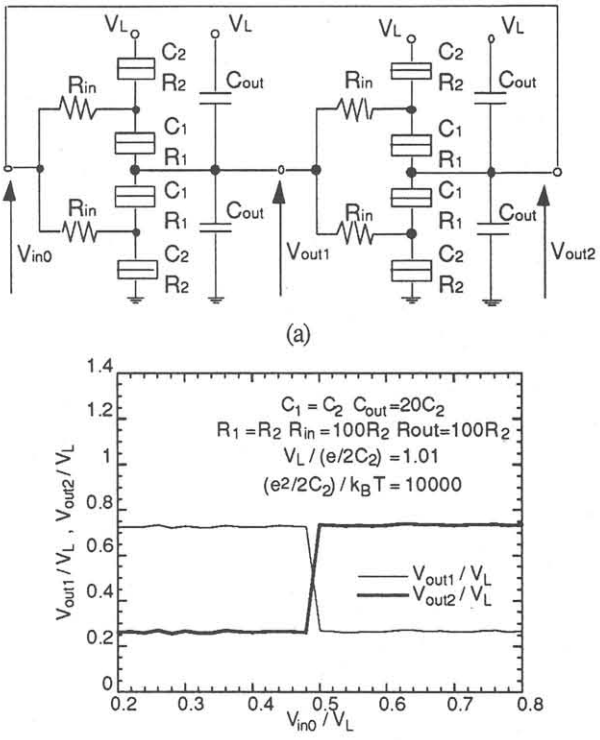

Fig. 7. (a) Cross-coupled latch circuit using the complementary R-SET inverter. (b) Time average of the output node voltages of the cross-coupled latch circuit. V_{in0} is an initial input node voltage.

5. Conclusion

We proposed a new complementary digital logic based on the resistively coupled single-electron-transistor and investigated its basic characteristics numerically using the Monte Carlo method. The complementary R-SET logic is thought to be advantageous in realizing a large scale digital logic circuit because the logic threshold is independent on the back ground polarization charges. It is shown from the calculation that the amplitude of the output voltage swing is about twice as large as the conventional resistance load R-SET logic, resulting in larger stability of the logic level. By calculating the transient characteristics, the switching time constant of the gate is estimated to be $530RC$, where R and C are the resistance and capacitance of the tunnel junction.

References

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