Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 210-212

Bistable Locking of Single-Electron Tunneling Junctions for Digital Circuitry

R. A. Kiehl and T. Ohshima

Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

Bistable phase-locking of single-electron tunneling oscillations is proposed as the basis for digital logic circuitry. A simple model of single-electron tunneling is used to examine the locking of capacitively coupled junctions pumped at twice the single-electron tunneling frequency and activated by clocking the dc bias. The results show that under these conditions the junctions exhibit locking properties potentially useful for digital circuitry in which the logic state is represented by binary phase states.

1. INTRODUCTION

A number of interesting proposals have been made for exploiting single-electron effects in ultra-small junctions as a basis for computation. These include circuits in which coulomb blockade is used to produce devices with transistor-like characteristics[1] [2] and circuits that encode digital bits of data with single electrons[3]. In addition, a scheme based on the bistable charge polarization caused by coulomb interaction in a two electron cell has been proposed[4].

2. BASIC DESCRIPTION

We propose a new approach to digital circuitry based on phase bistability in locked single-electron tunneling oscillations. The phase locking characteristics of elements comprised of capacitively coupled single-electron tunneling junctions pumped at twice the tunneling frequency and activated by clocking the dc bias are analyzed below. We show that single-electron tunneling events in such elements can be synchronized with the pump to produce a phase bistability having characteristics that make it potentially useful for digital logic circuitry in which logic states are represented by two stable phase conditions of single-electron tunneling, as illustrated in Fig. 1.

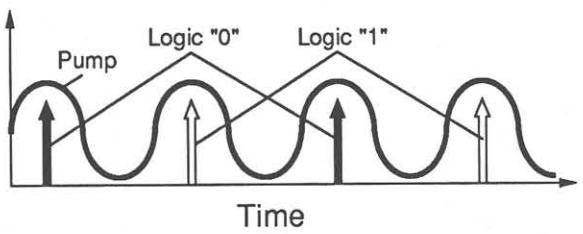

FIG. 1. Logic states defined by a locked single-electron tunneling process. In each of the two states, a single electron tunnels (arrows) at alternate peaks in the ac pump cycle. The logic state is represented by the phase of the locked tunneling process with respect to the pump.

2. MODEL

To examine the basic characteristics of this scheme, we carry out an approximate quasiclassical analysis in the low temperature limit using a deterministic model in which a particular single-electron tunneling event takes place as soon as it decreases the electrostatic energy of the system[3]. Accordingly, the junction voltage V_j is related to charge by the sawtooth characteristic $V_j(Q) = (Q-ne)/C_j$ for $(n-1/2)e \leq Q < (n+1/2)$ with integer n, where Q is the integral of the total current through the junction and e is the electron charge.

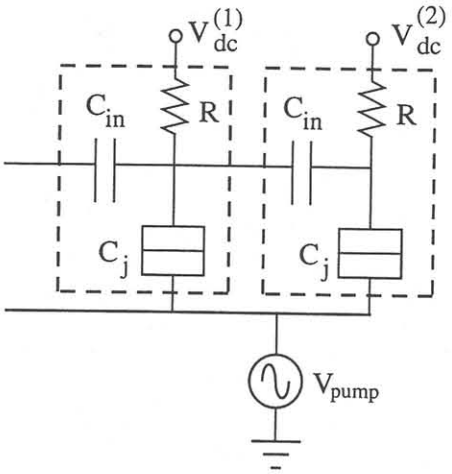

FIG. 2. Circuit diagram of two coupled stages. Tunnel junctions (double-box symbols) with capacitance Cj are pumped by a common ac source Vpump and dc biased by clocked sources Vj through a load resistance R. Stages are coupled by a capacitance Cin with a series resistance Rin (not shown).

We consider a circuit in which tunnel junctions with capacitance C_j are connected to a common pump signal V_{pump} coupled by a capacitance C_{in} and biased through a resistance R by a voltage source V_{dc}, as shown in Fig. 2. The tunneling resistance is assumed to be negligible compared with R. The coupling capacitance is taken to have a series resistance R_{in} since this is convenient for handling the redistribution of charge after tunneling. However, the results are insensitive to R_{in} for our choice of parameters. The pump is an ac voltage source V_p

$\cos(2\omega_S t)$ operated at twice the intended signal frequency ω_S. The pump supplies the drive for phase locking the oscillations and provides the circuit timing reference.

The basic operating principle is the generation of single-electron tunneling oscillations at ω_S that are phase locked to the pump, thereby creating a bistability due to the indeterminate phase relationship between the ω_S oscillation and the $2\omega_S$ reference. During operation, the n^{th} stage is clocked on by ramping its dc bias $V^{(n)}_{dc}$ from zero to a constant value. Operation so as to allow one junction to lock another would normally be performed by sequentially clocking stages, as in a conventional multiphase clock scheme. Thus, within this clocking scheme, the dc biases are clocked while the pump runs continuously.

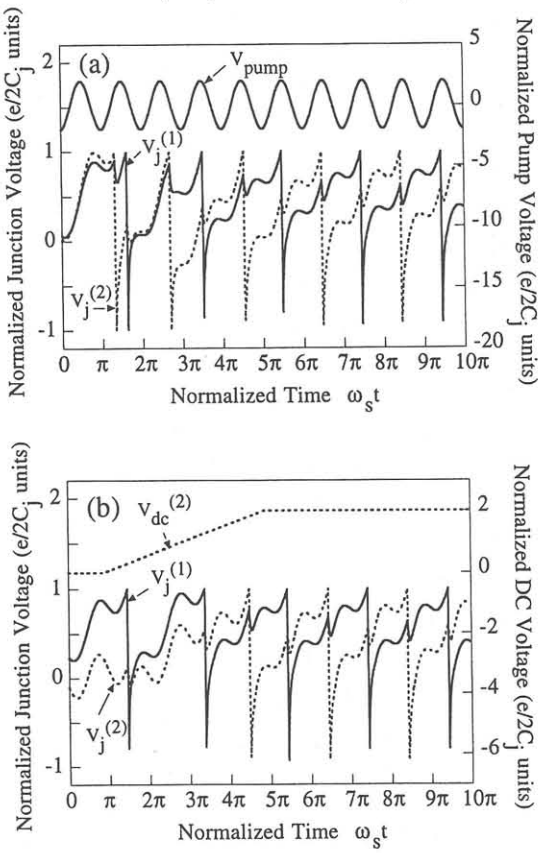

FIG. 3. Tunnel junction voltages Vj(n) and pump voltage Vpump versus time for two-stage circuit with (a) both stages clocked together and (b) the second stage clocked after the first. V(2)dc is the dc bias ramp for J2. Parameters a, b, e, g, and k are 2.0, 2.0, 0.5, 1/3, and 0.1.

3 SIMULATION RESULTS

We have investigated the locking of an individual stage to a sinusoidal input signal $V_{in}\cos(\omega_S t+\phi_{in})$ when the stage is activated by applying a step in the dc bias. The factor ϕ_{in} specifies the phase of the input signal with respect to the pump. The clock timing is similarly defined by the phase of the dc bias step ϕ_{clock}. (It should be noted that both ϕ_{in} and ϕ_{clock} are defined with respect to a cycle at ω_S.) The results show that the final state is controlled by ϕ_{in} regardless of the clock phase. Thus, there is an input amplitude threshold for control of the phase state. Above this threshold, the control mechanism exhibits noise margins with respect to the input signal phase, which is an essential feature for digital circuitry. Detailed results of this part of the calculations will be presented elsewhere.

Here we consider the locking of coupled stages. We consider the two-stage circuit in Fig. 2 with the input loaded by a capacitance C_j. Assuming slightly different initial conditions to unbalance the two elements, we apply a step in bias to both stages at once while the pump runs continuously. As shown in Fig. 3, the voltages rise together toward the critical tunneling voltage, $e/2C_j$, until an electron tunnels in the right-hand junction, J_2. As soon as the first electron tunnels in J_2, $V_j^{(1)}$ drops due to the redistribution of charge among the capacitances and then increases as J_1 continues to charge. The increase in $V_j^{(1)}$ is rapid because the pump voltage is rising, and an electron soon tunnels in J_1. Although the voltages across the junctions now rise together once again, J_2 now tunnels at a point in the cycle when the pump is falling. As a result, $V_j^{(1)}$ cannot reach the critical voltage until the following peak of the pump. Thereafter, the junctions lock in an antiphase relationship, where tunneling alternates back and forth between the junctions at successive peaks of the pump. Thus, a steady state is quickly reached in which tunneling in one junction suppresses tunneling in the other due to the charge redistribution and the fall of the pump.

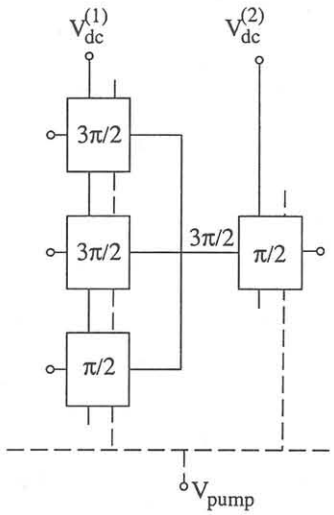

FIG. 4. Digital circuit based on majority logic. The outputs of three elements in stage (1) are summed to produce an input with the majority phase at stage (2). Sequential clocking of the stages controls the logic flow.

Now we examine the transfer of signals between sequentially activated stages. In this case, J_1 is biased first and allowed to reach steady state with $V^{(2)}_{dc}$ set to zero. Then, J_2 is clocked on by linearly ramping $V^{(2)}_{dc}$ to a constant value. A ramp duration equal to four cycles is used, and the response is calculated for different values of the clock phase f_{clock} in steps of $\pi/4$. Fig. 3(b) shows the response for ϕ_{clock} equal to $7\pi/8$. It can be seen that the first tunneling event in J_2 occurs out of phase with the oscillation in J_1, and the two junctions then lock rapidly in

antiphase with the phase of J_1 unchanged from its original state. For the parameters used here, this response is obtained over a large range of f_{clock} from $3\pi/8$ to $11\pi/8$. Over the remaining range of $13\pi/8$ to $\pi/8$, the junctions still lock in antiphase. In this range, however, tunneling in J_1 occurs early in the cycle (during the bias ramp) and the phase of J_1 is changed in the clocking process. Thus, the binary state can be transferred between two capacitively coupled stages by clocking the dc bias, provided that the clock phase is limited within a certain range by synchronization with the pump. In the present example, inverter-like operation, where sequentially clocked stages lock in alternate states, is obtained over the largest f_{clock} range. We have also obtained similar operation in the case of three coupled stages, where data is passed from two phase locked stages to a third stage by clocking.

4. CONCLUSION

The above properties are similar to those of the elements in the parametron digital circuitry proposed by von Neumann[5] and Goto[6]. Thus, our elements are potentially useful for analogous digital circuits. As in parametron circuits, digital information is represented by the phase-state of the oscillation and, hence, a single element such as shown in Fig. 1 can function as a basic memory cell. As in a parametron computer, logic may be performed using a majority logic scheme in which ac outputs from different stages are summed to produce a signal with the majority phase and logic flow is controlled by clocking signals from stage to stage[7], as illustrated in Fig. 4. In addition, the strong interaction between tunneling events in neighboring elements produces a spatial correlation of states which may be of use in other circuit architectures, such as cellular automata. Further study is underway to thoroughly investigate the operation of such circuits.

The authors would like to thank K.K. Likharev for commenting on this work and N. Fujimaki for his critical reading of the manuscript. The also gratefully acknowledge N. Yokoyama for his encouragement and support.

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