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Highly Reliable Ultra Thin Gate Dielectrics for Dual-Gate CMOS Devices

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Highly reliable ultra thin NO-nitrided SiO_2 has been demonstrated to be effective to suppress boron penetration for dual-gate CMOS applications. Boron-penetration-induced device instabilities (threshold voltage shift, increased subthreshold swing and enhanced short channel effect) are found to be alleviated in BF_2-implanted polysilicon gated p-MOSFETs with NO-nitrided SiO_2 as compared to control sample. After considering the excellent performance and reliability obtained in both n^+-poly n-MOSFETs and p^+-poly p-MOSFETs, NO-nitrided SiO_2 is concluded to be promising for dual-gate CMOS technology.

1. INTRODUCTION

Conventional p-channel MOSFETs which employ n^+-polysilicon gates typically require a compensating p-type channel implant to lower the native threshold voltage magnitude. This results in a buried-channel structure which is vulnerable to excessive short-channel effect caused by subsurface off-current conduction. Hence, in deep-submicrometer CMOS technology, p^+-polysilicon as the gate material for p-channel MOSFET has been proposed to improve short-channel behaviors [1]. One problem associated with this process is boron diffusion from heavily doped p^+-polysilicon through the thin gate oxide, causing undesirable device operation instability [2-3]. Previous studies have shown that NH_3-nitrided oxides and N_2O-based oxides can suppress boron penetration [4-8]. However, NH_3-nitrided oxides suffer from hydrogen-related electron trapping problem [9] and N_2O-based oxides do not have sufficient nitrogen concentration to effectively suppress boron penetration [5]. In this paper, we demonstrate the use of highly reliable NO-nitrided SiO_2 as the gate dielectrics of dual-gate CMOSFETs. NO process requires lower thermal budget and maintain the H-free nature of the processing ambient [10]. In addition to the enhanced boron diffusion barrier properties, significantly improved reliability characteristics have been achieved in NO-nitrided SiO_2 devices.

2. DEVICE FABRICATION

Dual-gates MOSFETs and MOS capacitors (p-type polysilicon for p-channel devices and n-type polysilicon for n-channel devices) were fabricated using CMOS twin-well technology. Gate oxides (control oxide) were thermally grown by dry oxidation in a conventional furnace. NO nitridation was performed in a RTP system with pure NO ambient at 1000°C for 10 sec (NO-oxide). The equivalent oxide thicknesses were ~63 for control SiO_2 and ~65.5 Å for NO-oxide. P-type polysilicon gate is BF_2-implanted with a dose of $5x10^{15}$ cm^{-2} at a energy of 25 KeV, whereas n-type polysilicon gate was phosphorus-implanted with a dose of $5x10^{15}$ cm^{-2} at an energy of 30 KeV. Both devices were subjected to oxide spacer formation and BPSG deposition at 800°C for 120 min, followed by a 900°C N_2 anneal (for both boron drive-in and BPSG densification) at different time (8, 18, 40, 60 min).

3. RESULTS AND DISCUSSION

A. Quasi-Static C-V Performance:

Fig. 1 shows the effect of the different N_2 drive-in time on quasi-static C-V curves of the p^+-polysilicon gated MOS capacitors with control SiO_2. With the increase of anneal time the C-V curve shifts to right, indicating severe boron penetration has occurred. However, similar phenomenon is not observed for NO-nitrided SiO_2. As shown in Fig. 2, for 900°C/60 min N_2 anneal, control SiO_2 with p^+-polysilicon gate shows much distortion and right-shift compared to NO-nitrided SiO_2. This distortion is attributed to boron penetration because n^+-polysilicon counterparts show very small difference among different samples.

B. Instability of MOSFET Performance:

The boron penetration in control SiO_2 degrades p^+-polysilicon gated p-MOSFET performance. As shown in Figs. 3 (a) and (b), the threshold voltage (V_t) and subthreshold swing (SS) of control sample increase with N_2 drive-in time. However, for NO-nitrided samples and for all n^+-polysilicon gated n-MOSFETs, V_t and SS are almost constant with respect to the different process condition. Therefore, NO-nitridation improves the process window for threshold voltage and subthreshold swing control of p^+-polysilicon gated p-MOSFETs. In addition, the degradation of p-MOSFET performance due to boron penetration becomes more severe if the channel length is reduced. As shown in Fig. 4, when the channel length is scaled from 10 μm to 1 μm, the "short-channel effect" is observed for control sample due to the reduced effective substrate doping concentration by the compensation of penetrated boron with n-well substrates. However, NO-nitrided sample still remain a normal behavior (*i.e.* without short-channel effect) due to their excellent diffusion barrier properties. It also should be noticed that in Fig. 4, the degradation of V_t and SS in the saturation region is much larger than in the linear region for control SiO_2, whereas NO-nitrided SiO_2 remain unchange. This further supports that the observed enhanced short-channel effect in control sample is due to the reduced net substrate doping because of severe boron penetration. Fig. 5 confirms that with the increase of boron penetration, the substrate net doping concentration does reduce significantly.

C. Channel Hot-Carrier Reliability of MOSFET

Channel hot-carrier immunity was monitored under the worst case stressing conditions (peak gate current $I_{g,peak}$ for p-MOSFET and peak substrate current $I_{sub,peak}$ for n-MOSFET). Fig. 6 (a) and (b) shows the change of threshold voltage and gate current for p^+-polysilicon p-MOSFET with control and NO-nitrided SiO_2 as a function of stress time at

fixed V_d and V_g-V_t, which corresponds to the $I_{g,peak}$ condition. Different drive-in times are used to investigate the influence of boron penetration on MOSFET reliability. It is found that in the control device with the increase of drive-in time, the threshold voltage significantly shifts after stressing due to severe electron trapping, as shown in Fig. 6 (a). Such behavior is mainly attributed to the larger gate current for buried-channel devices under identical stressing conditions [11]. Boron penetration results in a thin p-type layer formation under the SiO_2/Si interface, making the channel away from the surface. Since the position of maximal impact ionization is deeper in the buried channel device, the electron can pick up more energy in the transverse field, resulting in a higher gate current, as shown in Fig. 6 (b). On the other hand, the significant increase of threshold voltage shift (ΔV_t) and gate current is not observed in NO-nitrided devices. It is found that even with 60 min N_2 drive-in anneal, NO-nitrided SiO_2 device shows negligible ΔV_t. Therefore, it is believed that in addition to a stable performance resulting from p^+-polysilicon p-MOSFET with NO-nitrided SiO_2 gate dielectrics, an excellent channel hot-carrier immunity can also be obtained by using this efficient boron-stopping dielectric.

Fig. 7 plots the degradation in G_m for n^+-polysilicon n-MOSFETs with control and NO-nitrided SiO_2 as a function of stress time. The stressing is performed under the $I_{sub,peak}$ condition. It is found that NO-nitrided device shows negligible degradation of peak-G_m as compared to control sample, consistent with our previous finding for devices with thicker oxides (~150 Å) [10]. The strengthened interfacial characteristics of NO-nitrided SiO_2 through N incorporation is believed to be responsible for this improvement.

4. CONCLUSION

We have demonstrated that ultrathin NO-nitrided SiO_2 can be used in dual-gate CMOSFETs to alleviate the boron-penetration-induced device instability in BF_2-implanted polysilicon gated p-MOSFETs. In addition, excellent hot-carrier reliability has also been obtained in both n- and p-MOSFETs with NO-nitrided SiO_2 as compared to control samples. It is concluded that NO-nitridation technique is very promising for the incoming deep-submicrometer dual-gate CMOS technology.

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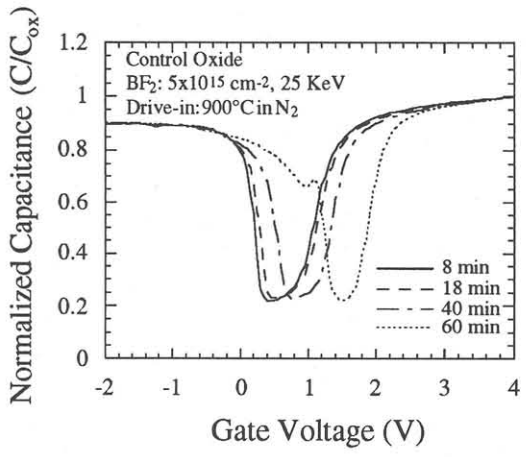


Fig. 1 Normalized quasi-static C-V curves for p^+-poly p-MOS capacitors with control SiO_2. The drive-in anneal was performed at 900°C in N_2 for different time.

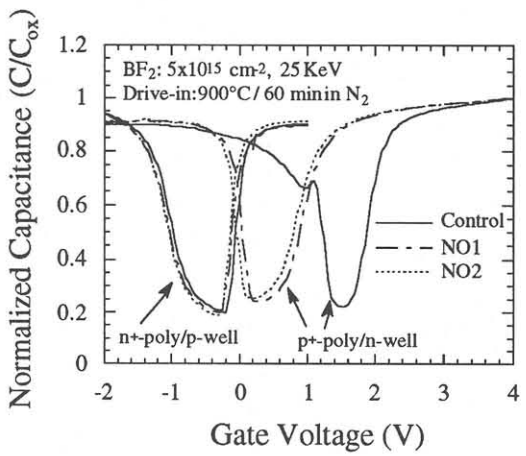
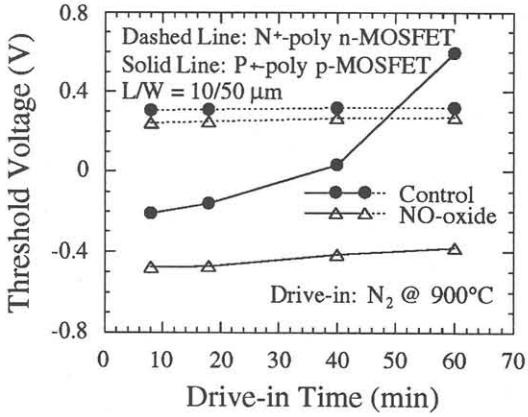


Fig. 2 Normalized quasi-static C-V curves for both p^+-poly and n^+-poly MOS capacitors with different gate dielectrics. The drive-in anneal was performed at 900°C in N_2 for 60 min.



(a)

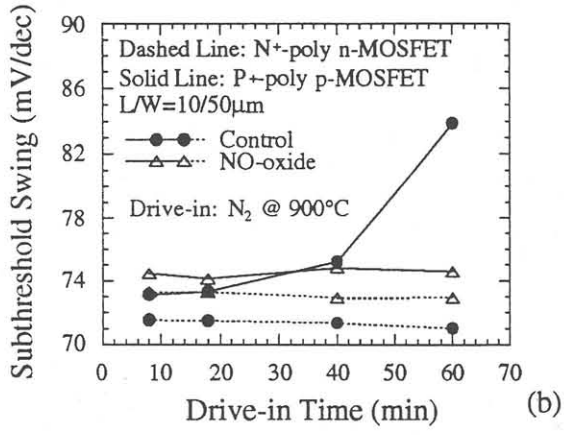


Fig. 3 (a) Threshold voltage and (b) subthreshold swing of dual-gate CMOSFETs with different gate dielectrics as a function of drive-in time. The drive-in anneal were performed at 900°C in N_2.

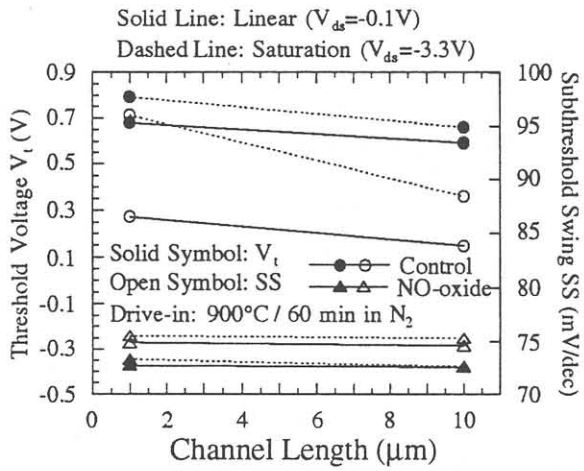


Fig. 4 Threshold voltage and subthreshold swing of p^+-poly p-MOSFETs with different gate dielectrics as a function of channel length. Both linear and saturation regions were studied.

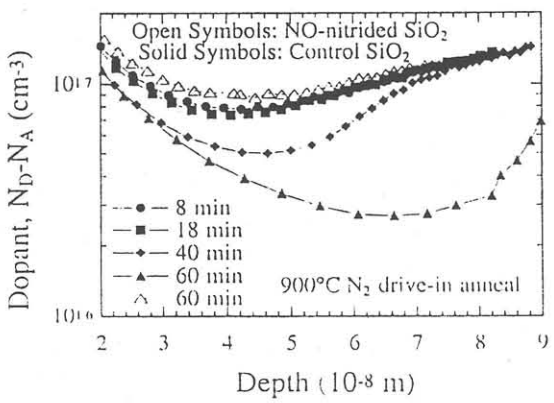
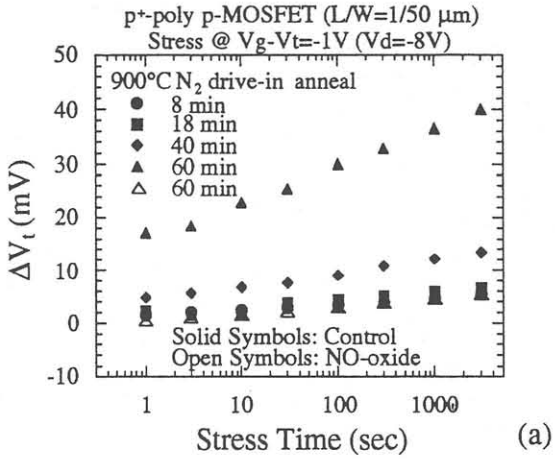


Fig. 5 The measured net channel dopant concentration N_D-N_A as a function of depth in p^+-poly p-MOS capacitors with different gate dielectrics. The doping profile was extracted from the measured high-frequency C-V curves. Note that there exists a limitation of the C-V technique at the distance about 2 ~ 3 Debye lengths from the SiO_2/Si interface.



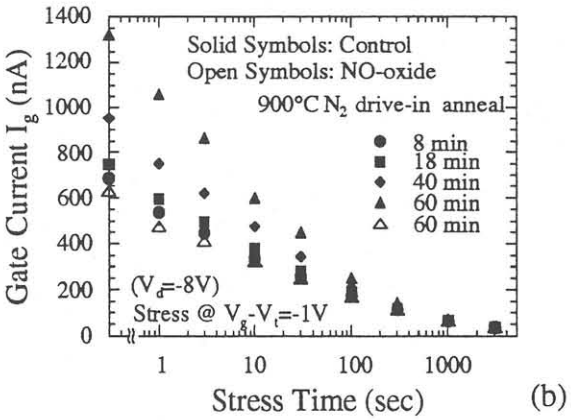


Fig. 6 (a) ΔV_t and (b) I_g for p^+-poly p-MOSFET with control and NO-nitrided SiO_2 as a function of stress time at fixed V_d (=-8V) and V_g-V_t (=-1V), which corresponds to the $I_{g,peak}$ condition.

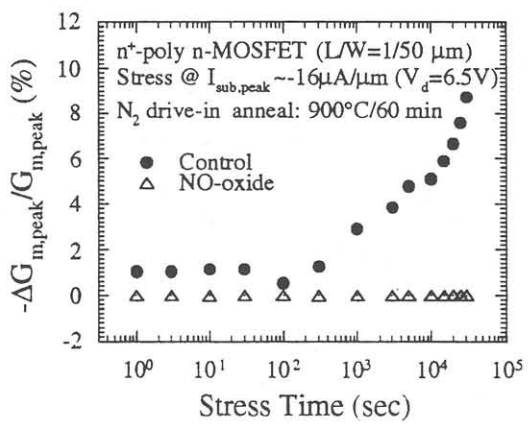


Fig. 7 Degradation in G_m for n^+-poly n-MOSFET with control and NO-nitrided SiO_2 as a function of stress time. The stressing was performed under the $I_{sub,peak}$ condition with V_d = 6.5 V.