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Dynamics of Hot-Carrier Induced Interface State Generation in Polysilicon Thin-Film Transistors

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Interface state creation, induced by hot-hole injection, has been frequently observed in n-channel polysilicon TFTs, when subjected to prolonged bias-stress with negative gate biases. In this letter we propose a new model for the kinetics of interface state formation, that closely links the interface state generation to the measured gate leakage current. The interface generation mechanism appears to be driven by the recombination of hot-holes (injected from the semiconductor active layer) with electrons (injected from the gate electrode). This model is shown to fit very well the time evolution of the interface states, as determined by the sheet conductance of the damaged region close to the drain.

1. INTRODUCTION

The effects of hot-carriers in polycrystalline silicon (polysilicon) thin-film transistors (TFTs) have been recently investigated, both in n-channel[1-6] and p-channel devices[7,8], in view of the application of such devices in active matrix LCD driving circuitry or SRAMs. In particular, the injection of hot-holes in n-channel devices has been observed to cause two effects: off-current reduction and transconductance degradation[3-5]. The first effect has been related to the formation of oxide traps that are charged positively[3-5]. The second effect is thought to be related to the formation of interface states and has been shown to strongly depend upon the concomitance of hot-hole injection, from the polysilicon active layer, and electron injection into the oxide, from the gate electrode[9,10]. Indeed, we have observed an increase of the transconductance degradation for increasing gate leakage current[10], confirming the relation between gate leakage current and interface state generation. In the present work we have studied the kinetics of interface state generation and a close link between interface trap density and gate leakage current is proposed.

2. DEVICE FABRICATION

The polysilicon TFTs were fabricated with a four mask sequence. The active layer (100 nm thick) was deposited amorphous by pyrolysis of Si_2H_6 in a UHVCVD reactor[11] and subsequently furnace-crystallised at 580°C. After definition and reactive ion etching (RIE) of the active polysilicon islands, the gate SiO_2 was deposited to a thickness of 120 nm by distributed electron cyclotron resonance plasma enhanced CVD[11]. The gate electrode was defined by a RIE etch of an in-situ doped amorphous silicon layer deposited by LPCVD at 560°C. The self-aligned source and drain contacts were formed by a phosphorous implant, which was activated by a furnace anneal at 580°C. This thermal treatment also converted the amorphous gate material to low resistivity degenerated polycrystalline silicon. The contacts were defined by lift-off of an evaporated aluminum film and the device were then annealed at 450°C under flowing forming gas (10% H_2 in N_2). This treatment is necessary to passivate silicon dangling bonds at the active polysilicon/SiO_2 interface[12]. Finally, the samples were covered with a SiO_2 passivation layer. We emphasize that the field-effect mobility in these devices, without post-hydrogenation treatment and with a maximum processing temperature of 580°C, is around 70 cm^2/Vs [13]. The device geometry used for the present experiments is: channel length 5 μm (L) and channel width 40 μm (W).

3. RESULTS AND DISCUSSION

Application of prolonged bias stress with negative gate bias (< -20 V) and high V_{ds} (20 V) have been shown to degrade the on characteristics of n-channel TFTs[10], as a consequence of the formation of interface states close to the drain junction[3-5]. The region where the interface defects are localized extends around 100 nm from the drain junction, as determined by our two dimensional device analysis performed with the program HFIELDS[4], and also in agreement with previous numerical results on c-Si MOSFETs[14]. Therefore, the sheet conductance of the stressed device can be viewed as resulting from the series of two channel regions: a damaged region (extending over d=100 nm) and the other having the same properties of the unstressed device (extending over L-d)[3]. In the unstressed device (uniform channel) we can define the normalized sheet conductance (G_1), measured at low V_{ds} (0.1 V), as:

$$G_1 = I_{d1} L / (V_{ds} W) \qquad (1)$$

where I_{d1} is the measured drain current. After stressing, the normalized sheet conductance of the damaged region (G_2) can be expressed as:

$$G_2 = (d/W) [V_{ds}/I_{d2} - V_{ds} (L-d) / (L I_{d1})]^{-1} \qquad (2)$$

where I_{d2} is the drain current measured in the stressed device at the same V_{ds}. In Fig. 1 the normalized sheet conductance of the damaged region is shown before and after different stressing times, with bias-stress conditions of V_g=-25

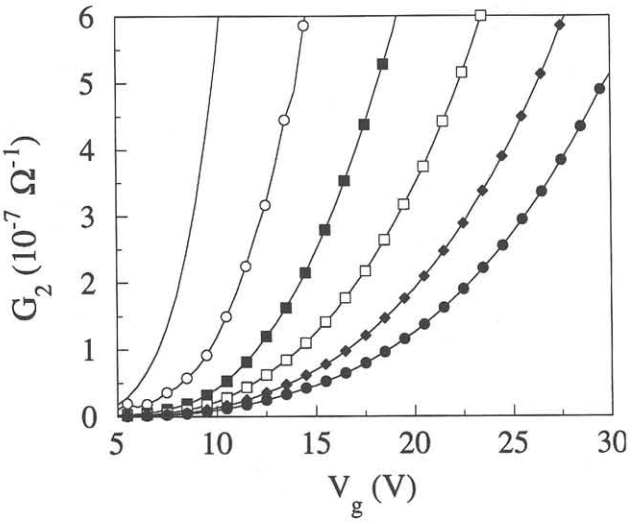

Fig. 1: Sheet conductance of the damaged region, G_2, obtained using the deconvolution procedure described in the text, versus gate voltage, V_g, before stress (continuous line) and after different stressing times (stress conditions fixed at V_g=-25V and V_{ds}=20V): (o) 60 s; (■) 420 s; (□) 3780 s; (◆) 15300 s; (●) 43200 s.

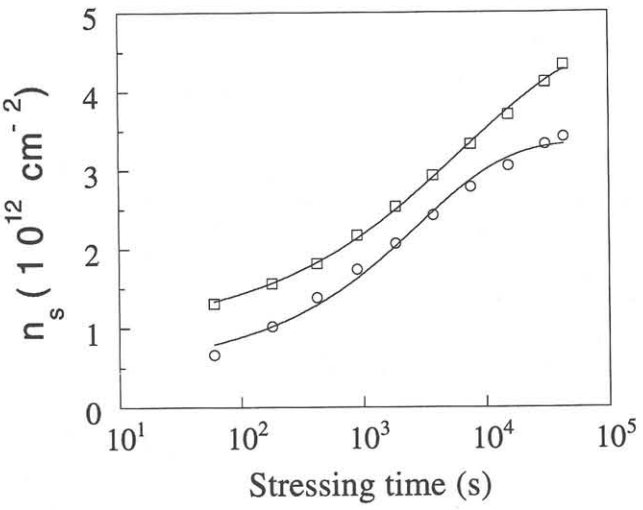

Fig. 2: Interface states generated during bias-stress versus stressing time for two different bias-stress conditions: (o) V_g=-25 V and V_{ds}=20 V; (□) Vg=-35V and V_{ds}=20V. Also shown are the fits to equation (5) (continuous lines).

V and V_{ds}=20V. As can be clearly seen, the on-regime is strongly affected by the bias-stress. It is worth to point out that the deconvolution procedure allow us to directly estimate the number of the generated interface states by analysing the sheet conductance of the damaged region , since in this region the interface state density can be reasonably assumed to be spatially uniform. In order to estimate the interface state density induced by the hot-hole injection, we can simply evaluate, after stressing, the excess applied gate voltage (ΔV_g) which is necessary in order to keep a constant G-value. Then, the number of interface states, n_s, that have to be filled to have the same band bending in the semiconductor is:

$$n_s=\Delta V_g C_{ox}/q \qquad (3)$$

where C_{ox} is the gate oxide capacitance per unit area and q is the unit charge. In Fig. 2 a plot of n_s, deduced for a constant G value of $5x10^{-7}$ Ω^{-1}, vs the stressing time is shown for two different bias-stress conditions.

It has been shown[10] that increasing the stressing negative gate bias below -20 V produces the generation of an increased number of interface states. This effect has been seen to be concomitant to an increased gate leakage current[10]. Indeed, as shown in Fig. 3 the gate leakage current, measured during the bias-stress, is higher at higher negative gate bias. It should be pointed out that even injecting into the gate oxide a considerable amount of hot-holes at stressing -10 V>V_g>-20 V (as evidenced by two orders of magnitude off-current reduction) g_m was not appreciably degraded in absence of an appreciable gate leakage current[10]. This substantiate the fact that hot-hole injection alone is not enough to efficiently generate interface states. The gate leakage current is likely to be due to electrons injected by Fowler-Nordheim mechanism from the polysilicon gate into the gate oxide, an increase in the gate-to-drain voltage clearly induces a substantial increase in the gate leakage current. In addition, it has also been shown that high-field constant current stress in c-Si MOS devices produces, when injecting electrons from the gate, a high rate of interface state generation at the Si/SiO_2 interface[15,16]. The collecting electrode interface appears to be the critical degradation site, where energetic electrons can release energy recombining with holes [15].

In order to correlate the gate leakage current with the phenomenon of interface state generation, we assumed that the interface state generation rate was proportional to the gate leakage current itself,J_L:

$$dn_s/dt= K J_L [N_s-n_s] \qquad (4)$$

where N_s is the interface state density at t=∞ and K is a constant. Solution of the differential equation (4) gives

$$n_s(t)= N_s [1-\exp(-KQ(t))] \qquad (5)$$

where $Q(t)=\int J_L dt$.

We then fitted the experimental $n_s(t)$ data, obtained from the sheet conductance deconvolution procedure, with eq. 5, where the experimental values of J_L were used to evaluate Q. As can be observed in Fig. 2 a very good agreement with the model is found for $N_s=3.34x10^{12}$ cm^{-2} for stressing at V_g=-25 V and $N_s=4.6x10^{12}$ cm^{-2} for stressing at V_g=-35 V. This confirms that the interface state generation is driven by the simultaneous injection of hot-holes (from the semiconductor active layer) and electrons (from the gate electrode), representative of the gate leakage current. In particular, the interface state generation mechanism could be explained in terms of electron-hole recombination at the insulator/semiconductor interface, as proposed by Lai[17]. Strained Si-O bonds at the insulator/semiconductor interface can be broken by the energy released by the electron-

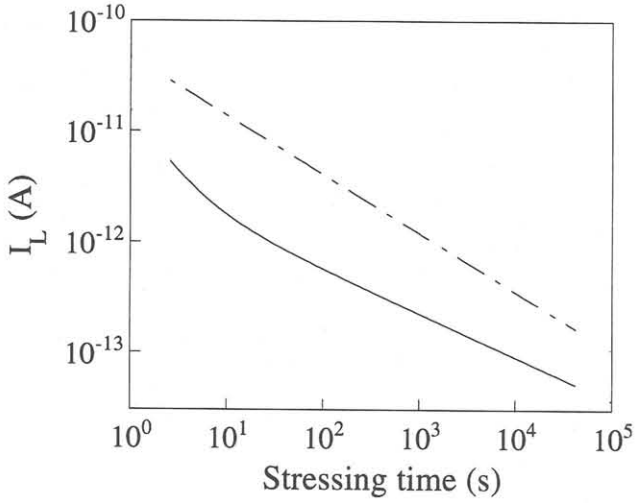

Fig. 3: Gate leakage current versus stressing time measured for two different bias-stress conditions: V_g=-25V and V_{ds}=20V (continuous line); V_g=-35V and V_{ds}=20V (dashed line).

hole recombination process and, subsequently, the O-atom can move to a lower strain position[17]. We note that during the electron-hole recombination process, occurring at the Si/SiO_2 interface, the energy released could be of the order of the SiO_2 band gap, since the hot-hole would be trapped first on Si-O strained bond and subsequently recombined with and electron injected into the SiO_2 conduction band from the polysilicon gate. Alternatively, the interface states could be generated by the breaking, induced by the energy released by the electron-hole recombination, of Si-H bonds[18], formed at the interface during post-metallization anneal. Both processes produce singly occupied silicon dangling bonds, that act as acceptor-like interface states. The precise determination of the microscopic mechanism behind the interface state generation is, however, beyond the scope of this work.

4. CONCLUSIONS

The evolution of interface state creation, induced by hot-hole injection, has been quantitatively studied in n-channel polysilicon TFTs. The generation mechanism has been observed to be driven by the simultaneous injection of hot-holes (from the semiconductor active layer) and electrons (from the gate electrode). In this framework, we have proposed a new model for the kinetics of interface state formation that closely links the interface state generation to the measured gate leakage current. This model has been shown to fit very well the time evolution of the interface states, as determined by the variation of the sheet conductance of the damaged region close to the drain.

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