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An Accurate Impact Ionization Current Model for LDD SOI MOSFETs

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Impact ionization phenomenon in submicron LDD SOI MOSFETs is investigated using devices with body terminals. It is shown that an accurate model for the impact ionization current in submicron LDD SOI MOSFETs has to account for the voltage drop on the parasitic source-and-drain and body series resistances, the gate-voltage dependent saturation field in the expression for the maximum channel electric field E_m and the self-heating effect. It is demonstrated that the plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ is a single straight line for a given technology.

1 Introduction

Recently power-performance advantage of SOI CMOS over bulk for low-power applications has been demonstrated and technology commercialization has become possible [1]. One of the greatest barriers to the introduction of SOI has been the floating body effect. Floating-body potential reduces SOI device threshold voltage and causes kink, single device latch and early breakdown. Therefore, an accurate models for the floating body effects in SOI are of great importance for optimum circuit design. However, the conventional model for impact ionization current [2], [3], based on the assumption that $ln(I_{IMP}/(I_D(V_D - V_{DSAT})))$ versus $1/(V_D - V_{DSAT})$ is a single straight line for a given technology, yields significant errors, which are manifested as deviation of the plot from a single straight line [4]-[5]. The deviation is caused by the influence of the source-and-drain and body parasitic series resistances and inaccuracy of the approximations [2], [3] for the maximum channel electric field in submicron channel length devices. In addition, the self-heating effect has to be accounted for. Using SOI MOSFETs with body terminals, we develop a new model for the submicron channel length LDD SOI devices.

2 Impact Ionization Current Model

Based on a quasi two-dimensional model [3], the maximum electric field is expressed as

$$E_m = \sqrt{(V_{DS} - V_{DSAT})^2/l^2 + E_{SAT}^2}, \qquad (1)$$

where l is the effective length of the saturation region. In order to account for the gate-voltage dependence of the saturation electric field we express E_{SAT} by the relationship [6]

$$E_{SAT} = 2V_{MAX}/\mu_{eff} \qquad (2)$$

where V_{MAX} is the maximum velocity of the carriers, μ_{eff} is the effective mobility,

$$\mu_{eff} = \mu_0/[1 + \theta(V_{Gf} - V_T)], \qquad (3)$$

V_{Gf} is the front-gate voltage and θ is the mobility degradation factor. We use the following well-known expression for the impact ionization current [2]:

$$I_{IMP} = A/B\ l\ E_m I_D \exp(-B/E_m), \qquad (4)$$

where A and B are assumed to be known constants and the saturation voltage is determined as:

$$V_{DSAT} = \frac{(V_{Gf} - V_T)E_{SAT}L}{(V_{Gf} - V_T) + (1 + \alpha + \gamma)E_{SAT}L}, \qquad (5)$$

where α accounts for charge coupling between the front and back gates, γ for the drain-induced conductivity enhancement as described in [7], L is the effective channel length.

Reduction in the threshold voltage as a function of the body potential V_B is approximated as

$$\Delta V_{TH} = (\sqrt{2\epsilon_s q N_D}/C_{ox})(\sqrt{2\phi_p + V_B} - \sqrt{2\phi_p}). \qquad (6)$$

The temperature dependences

$$\mu_0(T) = \mu_0(T_0)(T_0/T)^{1.7}, \qquad (7)$$

$$V_{FB}(T) = V_{FB}(T_0) - (1.2 \times 10^{-3})T, \qquad (8)$$

$$V_{MAX} = V_{MAX}(T_0) - (2.3 \times 10^3)T, \qquad (9)$$

derived in [8], were used to account for the temperature effect. The temperature is assumed to be dependent on the device operating power:

$$T = T_0 + (I_D V_{DS})R_1 + (I_D V_{DS})^2 R_2, \qquad (10)$$

where T is the operating temperature, T_0 is the ambient temperature.

Application of the model requires the effective length of the saturation region l to be known. Same as in [2], [3] we treat l as a process dependent parameter which needs to be determined experimentally for each technology.

We express accuracy of the model by the sum of squares of impact ionization current measurement and simulation deviations over the range of applied drain and front-gate voltages:

$$\sum [I - I_{IMP}]^2 = \sum \left[I - \frac{A}{B} l E_m I_D exp\left(-\frac{B}{E_m}\right)\right]^2, \qquad (11)$$

where I and I_D are measured values of impact ionization and drain currents, respectively and impact ionization current is modelled by (4).

Parameter extraction for the developed model has been carried out in two steps. First, the saturation region effective length l was extracted by the Levenberg-Marquardt numerical method using measurements for V_D less than 3 V in the low power area of device operation, where the temperature rise can be considered to be negligible. Parameters of the operating temperature dependence (10) and body resistance were extracted using I_B and I_D measurements for V_D in the range 3 V - 4.2 V, using the fact that voltage drop on the body resistance is negligible for higher front-gate voltages.

3 Experimental results and discussion

The developed model was applied to LDD SOI MOSFETs with gate width $W = 10\mu m$ and the effective channel lengths $L = 0.32;\ 0.52;\ 0.72\ \mu m$. The gate oxide thickness was 15 nm and the silicon film thickness was 100 nm. All SOI MOSFETs have body terminals. Low-field mobility is $\mu_0 = 570\ cm^2/(V\,s)$ and mobility degradation factor is $\theta = 0.232\ V^{-1}$. Gate-voltage-dependent parasitic source and drain series resistance was extracted and approximated by the relationship $R_{DS}[V_{Gf} - V_T] = 567(V_{Gf} - T_T)^{-0.88}\ \Omega$ (Fig 1). In Fig 2 a plot of $I_{IMP}/(I_D(V_D - V_{DSAT}))$

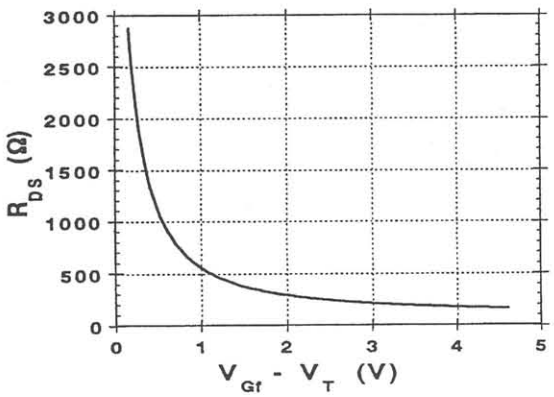

Figure 1: The extracted parasitic source-and-drain series resistance

versus $1/(V_D - V_{DSAT})$ is shown, where $V_D = 3V$ is the drain-source voltage applied to the SOI MOSFET. Series of almost parallel curves are obtained and therefore the conventional model [2], [3], based on the assumption that the above mentioned plot is a single straight line for the whole range of applied drain and gate voltages, is unapplicable. First, we investigate the influence of the parasitic source and drain series resistances. In Fig 3 a plot of $I_{IMP}/(I_D(V_D - V_{DSAT}))$ versus $1/(V_D - V_{DSAT})$ is shown, where V_D is now the voltage, applied to the intrinsic SOI MOSFET. The *intrinsic* voltages were calculated as: $V_{D(int)} = V_D - I_D R_{DS}[V_{Gf} - V_T]$ and $V_{Gf(int)} = V_{GS} - I_D R_{DS}[V_{Gf} - V_T]/2$. When the conventional model [2], [3] is applied for the *intrinsic* voltages the measurement data fall approximately on a single straight line for lower $1/(V_D - V_{DSAT})$, but deviate

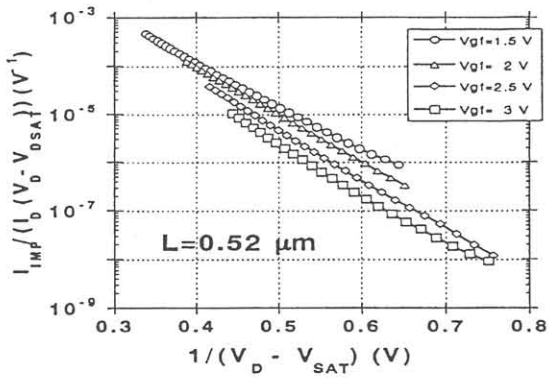

Figure 2: Plot of $I_{IMP}/(I_D(V_D - V_{DSAT}))$ versus $1/(V_D - V_{DSAT})$ for extrinsic applied voltage

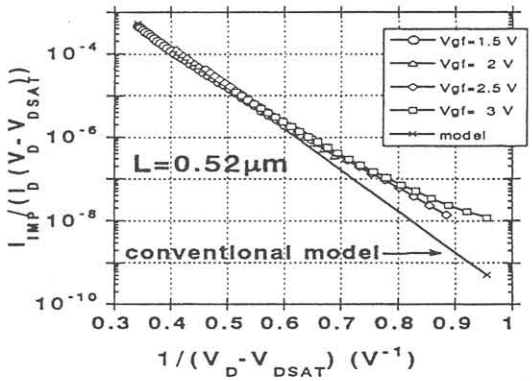

Figure 3: Plot of $I_{IMP}/(I_D(V_D - V_{DSAT}))$ versus $1/(V_D - V_{DSAT})$ for intrinsic applied voltage

from a single straight line for higher $1/(V_D - V_{DSAT})$, producing error of more than one order of magnitude. The deviation is explained by the front-gate voltage dependence of the saturation electric field. In Fig 4 a plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ is made, where E_m was calculated using (1) for the *intrinsic* voltages, and the data fall on a single straight line with good agreement between measurements and calculation.

The extracted values of the velocity-saturation region effective length l were 0.112 μm for $L = 0.32\ \mu m$, 0.132 μm for $L = 0.52\ \mu m$ and 0.150 μm for $L = 0.72\ \mu m$. Therefore, the effective length of the saturation region becomes gate-length-dependent for the submicron channel length devices.

Finally, when the plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ is made for V_D up to 4.2 V, deviation from a single straight line is observed in the higher electric field region as shown in Fig 5. The deviation is explained by the self-heating effect and the threshold voltage reduction due to body potential equal to the voltage drop on the drain voltage dependent body resistance. In Fig 6 the extracted parasitic body resistance and in Fig 7 calculated operating temperature are shown.

After voltage drop on the the body resistance and self-heating effect are accounted for, good agreement between measurements and simulation of impact ionization current is achieved (Fig 8).

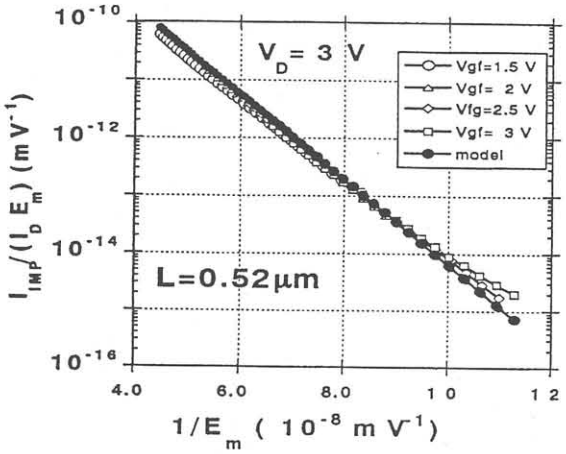

Figure 4: Plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ for intrinsic applied voltage

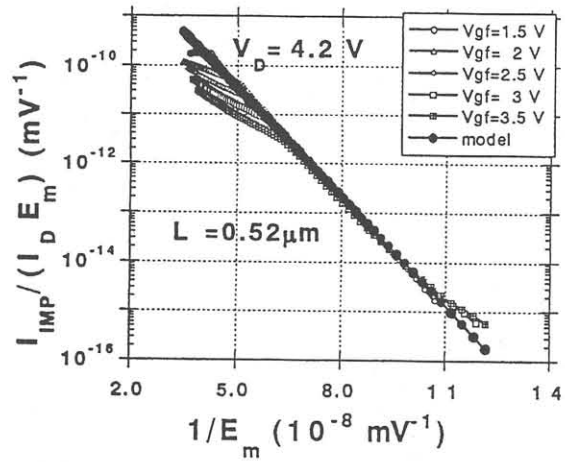

Figure 5: Plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ for V_D up to 4.2 V

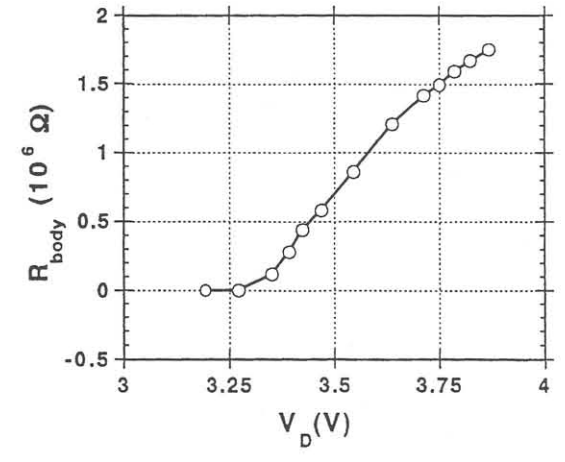

Figure 6: The extracted body resistance versus applied drain voltage

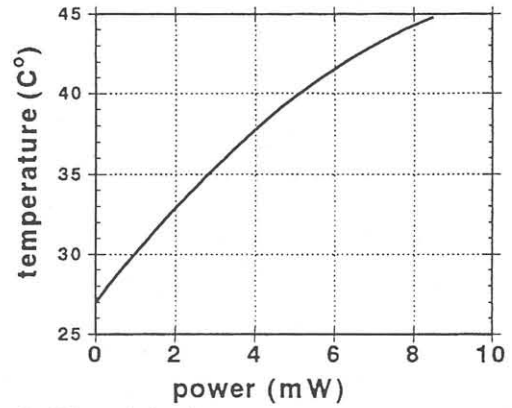

Figure 7: Plot of the device temperature versus the operating power

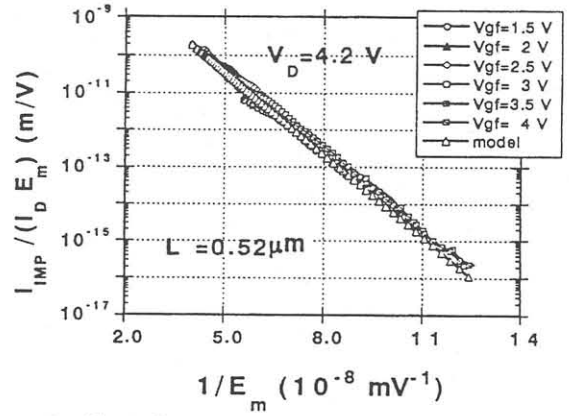

Figure 8: Plot of measured and simulated $I_{IMP}/(I_D E_m)$ versus $1/E_m$ for V_D up to 4.2V

4 Conclusion

It has been shown that an accurate model for impact ionization current in LDD SOI MOSFETs is obtained if voltage drops on the parasitic source-and-drain and body series resistances and the self-heating effect are accounted for and the gate-voltage dependence of the saturation electric field is included into the expression for the maximum channel electric field.

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