Advanced Quality in Epitaxial Layer Transfer by Bond and Etch-Back of Porous Si

Nobuhiko SATO, Kiyofumi SAKAGUCHI, Kenji YAMAGATA, Yasutomo FUJIYAMA, Jun NAKAYAMA, and Takao YONEHARA

Device Development Center, R&D Headquarters, Canon Inc.
6770, Tamura, Hiratsuka, Kanagawa, 254, Japan
e-mail: hiko@chcc.canon.co.jp

We report the recent qualitative advances in bond and etch-back SOI using structure-sensitive selective etching of porous Si. The defect density in the epitaxial layer on the porous Si is lowered to 3.5×10^2 /cm^2 by "pre-injection technique" in which a small amount of Si is supplied during high temperature H$_2$ prebake prior to epitaxial growth. H$_2$ annealing also smoothes the SOI surface comparable to the bulk polished wafer. The improved thickness uniformity of ± 1.8 % is achieved by the single wafer processing epi-reactor. The electrical characteristics is evaluated by pn-junction diode.

I. Introduction

SOI devices in the ultra thin films are a good candidate for high speed and low power applications such as wireless communication, DRAM, and MPU. The high crystalline quality and the small thickness variation in the SOI is required for large scale integration of the devices.

Bond and etch-back SOI (BESOI) has been developed since 1983, in which p⁻ epitaxial layer on p⁺ or p⁺/p⁻ substrate was bonded and was left on another handle wafer by etching back of p⁺ region, selectively[1-4]. In these dopant-sensitive etching systems, the etching selectivity is degraded by the doping profile broadening due to high temperature heat treatments both to grow the good epitaxial layer and to increase the bonding strength. Thus it is difficult to realize the good thickness uniformity by using the high temperature heat treatments.

Recently, we employed porous silicon for the new BESOI method, in which epitaxial layer on porous Si was transferred onto another handle wafer by bonding and etching back of porous Si (ELTRAN)[5-9]. In this novel method, the structure-sensitve selective etching, in which porous Si was etched by capillarity induced penetration, replaced the dopant-sensitive one. This achieved the good SOI thickness uniformity in thin film region (~100 nm $\pm$ 5 %) due to its extremely high etching selectivity (10^5) and also allowed high temperature processing (epitaxial growth and bonding annealing). The major crystalline defects were stacking faults with the density of $10^3 - 10^4$ /cm^2.

We have been throughout pursuing advances mainly in crystalline quality, surface micro-roughness through investigation of H$_2$ annealing effects. In addition, the SOI thickness uniformities are discussed and compared.

II. Defect reduction in epitaxial layers on porous Si

The epitaxial layers were grown by the following sequence. 10 μm-thick porous Si was formed by anodization of 5-inch (100) heavily boron doped ($0.01-0.02$ $\Omega\cdot$cm) Si wafer in 49%-HF + C$_2$H$_5$OH (2:1) solution. Porous Si was measured to have enormous surface to volume ratio of ~100 m^2/cm^3 by the BET gas adsorption method, and surface pore
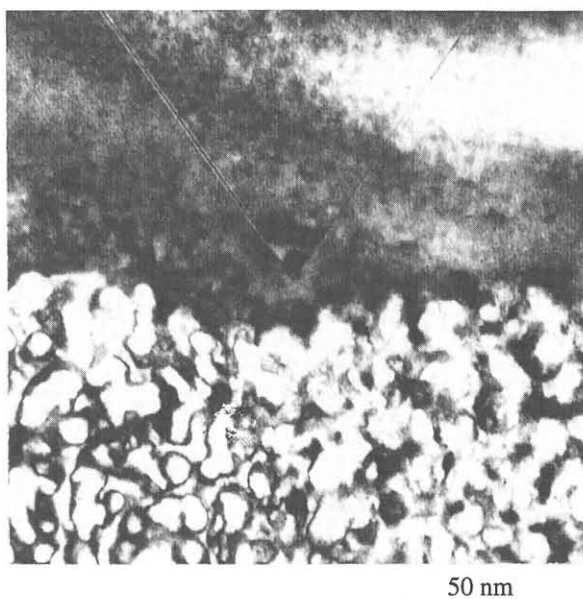
Fig. 1 A cross-sectional TEM micrograph of the epitaxial layer on porous Si. The V-shaped line in the epi-layer is a stacking fault pyramid. Note that the apex of the pyramid is not located just at the interface.
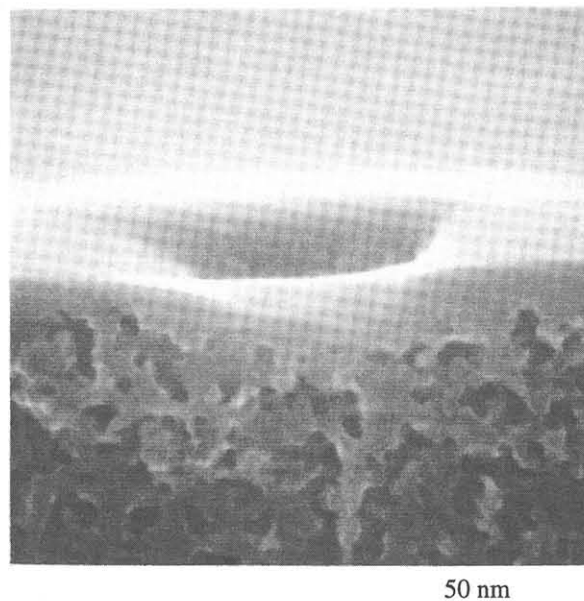
Fig. 2 A oblique view of high-resolution SEM micrograph of the H$_2$ prebaked porous Si. The prebaking condition is 1040 °C at at 760 Torr for 7.5 min. in H$_2$. The dimple indicates the residual pore.

density was ~10^{11}/cm² from SEM micrographs. Porous Si was slightly oxidized at 400 °C in dry O_2 ambient to cover pore walls which prevent from pore coarsening during the heat treatment such as epitaxial growth and bonding anneal. The serious structural modification without this preoxidation degrades the selectivity in structure-sensitive etching, however, the thin oxide at the porous surface would generate crystalline defects in the epitaxial layer. Therefore, the wafer was dipped in diluted HF for 30 seconds to remove the thin oxide only at the porous surface before loading into a CVD chamber, and H_2 prebake was also employed to remove the surface oxide of the porous layer. The epitaxial layer was grown by CVD just after the H_2 prebake.

To investigate the stacking-fault generation mechanism, the advanced thinning method using focused ion beam technique in conjunction with defect delineate etching was applied to observe the origin of the stacking fault by X-TEM as shown in Fig. 1. The interface between the epitaxial and porous layer is concave under the defect. The apex of the stacking fault pyramid is not located just at the interface but is included in the epitaxial layer at slightly upper portion from the interface.

H_2 prebaked porous Si was closely investigated by HR-SEM. The prebake filled up most of the surface pores, reducing the pore density from 10^{11} /cm² to the detection limit by SEM ($< 10^7$ /cm²)[6,9]. The pore filling is due to migration of Si atoms at the porous surface driven by surface energy minimization after removal of the surface thin oxide by HF dipping and H_2 prebake. One of the residual pores located at the dimple of the prebaked porous surface is shown in Fig. 2. Relatively large pores should be remained by the insufficient surface migration, or shortage of the surface Si atoms to fill up.

These observation suggests that the stacking faults are presumably generated just above the large residual pores during the initial stage of the growth. We tried two approaches to suppress the generation of the stacking faults by reducing residual pore density. One is to enhance the surface migration by raising the prebake temperature, and the other is to supply a small amount of Si flux during the surface migration (H_2 prebake) to fill up residual pores, "pre-injection", after removal of the thin oxide. As shown in Fig. 3, the stacking fault density was reduced to 1 x 10^3 /cm² by raising the prebake temperature up to 1150 °C. Further reduction was achieved by the pre-injection technique. It successfully reduced the defect density to 3.5 x 10^2 /cm² which represented the quite high SOI quality.
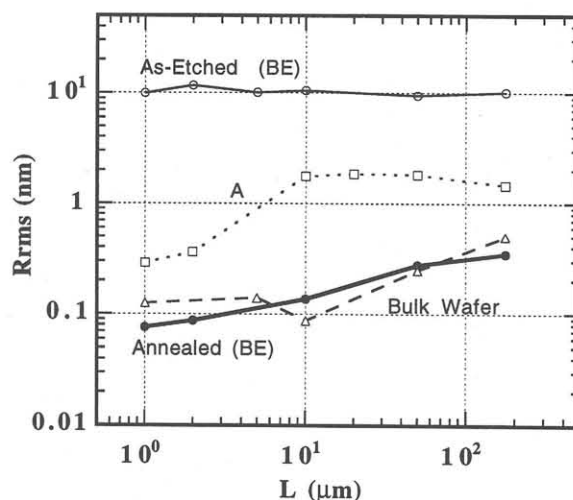
III. Surface micro-roughness

The above defect reduction technique also improved the surface micro-roughness of the epitaxial surface over the porous Si. The root-mean-square of the surface roughness (Rrms) was decreased from 0.7 to 0.2 nm in 50 x 50 µm², which is equivalent to that of the polished bulk Si wafer. This reduction in the surface roughness dramatically suppressed the void formation at the bonding interface.

The epitaxially grown surface of the prime wafer was thermally oxidized to reduce interfacial states and to keep away from the bonding interface which is easily contaminated with air-born boron, and was bonded with thermally oxidized handle wafer. The porous layer was exposed by grinding from the back side of the prime wafer, and was selectively etched off with extremely high selectivity of 10^5 in HF-H_2O_2. The as-etched surface was as rough as 10 nm in Rrms by AFM evaluation, reflecting the interfacial morphology between the epitaxial and the porous layer. This as-etched rough SOI surface was smoothed out again by annealing in H_2, reaching the very small surface micro-roughness comparable to commercially available bulk Si wafer in the wide range of measuring areas by atomic force microscopy as shown in Fig. 4. In the small scanning area, the atomical steps and terraces structure by (2x1) reconstructed surface were observed. In addition, boron in the epitaxial layer as high as 2 x 10^{18}/cm³ was simultaneously diffused out to <1 x 10^{16} /cm³ by the H_2 annealing[10]. In-situ removal of native oxide by the H_2 annealing plays an important role in these effects. The oxide acts as a barrier of the migration and the boron diffusion.
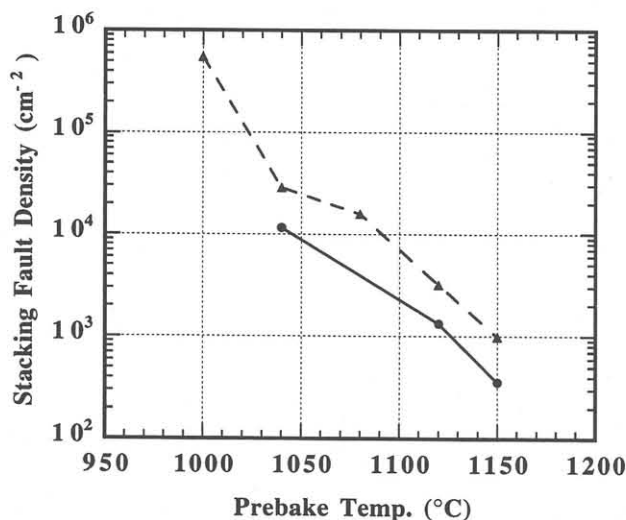
Fig. 3 Stacking fault density versus prebake temperatures. Epitaxial layers were grown at 760 Torr with SiH₂Cl₂ (250 sccm) in H_2 carrier gas after porous Si was prebaked in H_2 at 760 Torr for 7.5 min. The conventional method with no SiH₂Cl₂ during the prebake (triangles) and the new "pre-injection technique" (circles), in which a small amount of SiH₂Cl₂ (10 sccm) was supplied during the prebake, are plotted.

Fig. 4 Scanning area dependence of root-mean-square of the surface micro-roughness measured by atomic force microscopy. X-axis indicates a length of a side of a scanning square. As-etched (open circles), and H_2 annealed (closed circles) BESOI of this method, polished bulk Si wafer (open triangles), and oxygen ion implanted SOI wafer (open squares) surfaces were measured. The annealing condition was 1150 °C, 80 Torr, 1 h, in H_2.
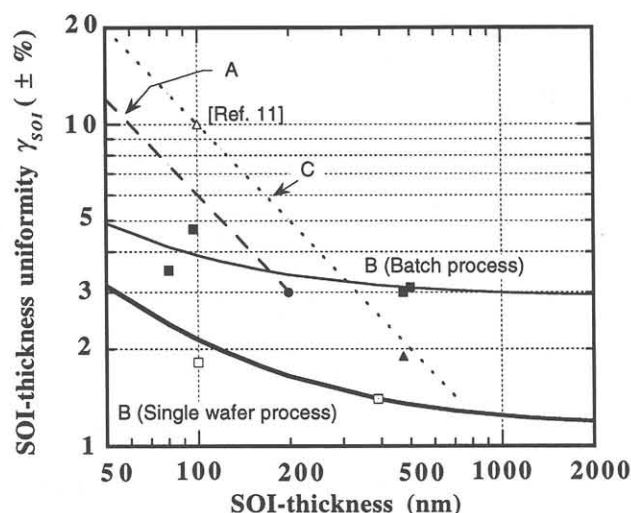
IV. Thickness uniformity

The final SOI thickness uniformity is determined by the three processes of the epitaxial growth, the selective etching of porous Si, and the final wet cleaning. In the epitaxial deposition, the ratio (γ_{epi}) of the variation to the grown thickness (t_{epi}) is constant. The batch process (barrel type reactor) gave the uniformity around ± 3-5 %[6], and the single wafer processing epi reactor improved the uniformity, as small as ± 1.6 % on the whole 5-inch wafer. The etching of porous Si with extremely high selectivity and the final wet cleaning process (SC-1 etc.) slightly degrade the thickness uniformity ± 1 nm at worst. Therefore, the ratio (γ_{SOI}) of the variation to the SOI thickness is difined by as follows.

$$\gamma_{SOI} \leq \gamma_{epi} + 1 \; (nm) \, / \, t_{epi}(nm)$$

Figure 5 shows the comparison of SOI uniformities formed by various methods in a function of the SOI layer thickness. The single wafer processing epi gave the better uniformity (γ_{SOI}) of this BESOI (98.7 nm ± 1.8 %).

The ratio (γ_{SOI}) of the variation are increased linearly as thinning the SOI layers by other methods. In the oxygen implantation method, the as-implanted variation is preserved after sacrifacial oxidation to thin the SOI thickness, so that the ratio (γ_{SOI}) increases when the thickness decreases. In the plasma thinning method, the variation of the plasma thinned thickness is hardly affected by the final SOI thickness in sub-μm region. The small thickness variation of this method was remarkable particularly in the thin film region. It is anticipated to reduce the threshold-voltage-shift in fully depleted MOSFETs.

Fig. 5 Comparison of thickness uniformities of the various SOIs in a function of SOI thickness. BESOI of this method by batch-process epi (closed squares), single-wafer-process epi (open squares), commercially available SOIs: A; oxygen ion implanted (circles), and C; plasma thinning (triangles) are indicated. The uniformities were evaluated from 97 points measurements in 5-inch whole SOI wafer surfaces.
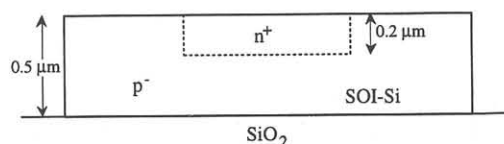
Fig. 6 Schematic illustration of pn-junction diode. The p⁻ region is boron-doped with 4×10^{16} /cm³.

V. Electrical characterization

I-V characteristics of the pn-junction diodes as shown in Fig. 6 was measured, and n-value in the following eqaution is evaluated for the bulk wafer and SOIs. The junction area is varied from $4.2 \times 10^2 - 6.4 \times 10^5 \; \mu m^2$.

$$I = I_0 \, exp(qV/nkT)$$

The average n-values from 39 points measurements are 1.01, 1.10 and 1.23 for the bulk, this BESOI with relatively high defect density ($\sim 10^4$/cm²), and the oxygen ion implanted SOI with additional epitaxial growth, respectively. The further improvement in n-value is anticipated for the latest BESOI of this method with the lower defect density ($\sim 10^2$ /cm²).

VI. Conclusions

We reported the recent qualitative advances in the BESOI (ELTRAN). The defect density in the epitaxial layer on the porous Si was decreased to 3.5×10^2 /cm², which was achieved by raising the H_2 prebake temperature, in conjunction with the pre-injection technique. H_2 annealing smoothed the resultant SOI surface comparable to the bulk polished wafer. The thickness uniformity was improved ± 1.8 % by the single wafer processing epi-reactor. The electrical property is being evaluated. The large-scale device integration would be feasible by these advances.

References

1) M. Kimura, K. Egami, M. Kanamori, and T. Hamaguchi, Appl. Phys. Lett. **43** (1983) 253.
2) J. B. Lasky, S. R. Stiffler, F. R. White and J. R. Abernathey, 1985 Int. Electron Devices Meeting Tech. Dig. pp. 684 (1985).
3) W. P. Maszara, G. Goetz, A. Caviglia and J. B. Mckitterick, J. Appl. Phys. **64** (1988) 4943.
4) C. E. Hunt and C. A. Desmond, *Proc. 1st Int. Symp. Semiconductor Wafer Bonding: Science, Technology, and Applications* **PV 92-7**, pp. 165 (The Electrochemical Society, Pennington, 1992).
5) T. Yonehara, K. Sakaguchi, N. Sato, Appl. Phys. Lett. **64** (1994) 2108.
6) N. Sato, K. Sakaguchi, K. Yamagata, Y. Fujiyama, and T. Yonehara, *Proc. of the 7th Int. Symp. on Si Mater. Sci. and Tech.* **PV 94-10**, pp. 443 (The Electrochemical Society, Pennington, 1994).
7) K. Sakaguchi, N. Sato, K. Yamagata, Y. Fujiyama and T. Yonehara, Jpn. J. Appl. Phys. **34** (1995) 842.
8) T. Yonehara, K. Sakaguchi, N. Sato, *Proc. 3rd Int. Symp. Semiconductor Wafer Bonding: Science, Technology, and Applications* (1995 May, Nevada), to be published.
9) N. Sato, K. Sakaguchi, K. Yamagata, Y. Fujiyama, and T. Yonehara, J. Electrochem. Soc. (1995), to be published.
10) N. Sato, T. Yonehara, Appl. Phys. Lett. **65** (1995) 1924.
11) P. B. Mumola, G. J. Gardopee, T. Feng, A. M. Ledger, P. J. Clapis, and P. E. Miller, *Proc. 2nd Int. Symp. Semiconductor Wafer Bonding: Science, Technology, and Applications* **PV 93-29**, pp. 410 (The Electrochemical Society, Pennington, 1992).