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Partially Bonded SOI Substrates for Intelligent Power ICs

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Abstract

A new SOI structure for intelligent power ICs was developed by using a wafer direct bonding technique. This structure has partial buried oxide films for dielectric isolation and gaps are fabricated under those buried oxide films. In this bonding technique, bonding surface is crystalline silicon surfaces of vertical output device region without buried oxide film region. This bonding method leads to void -free bonding at vertical output device region. The electrically perfect bonding was obtained for the vertical output device in the new structure.

1. Introduction

Intelligent power ICs having vertical double-diffused MOS (VDMOS) output devices are used for solenoid controlled application. It is difficult to fabricate SOI structures for these power ICs, because the buried oxide must be formed partially to permit the drain current of the VDMOS to flow vertically. Many structures have been proposed for these power ICs[1-4]. Ohoka et al. have proposed a direct bonded wafer having partial SOI structures for those intelligent power ICs[3]. But it is difficult to obtain void free structures. Hamajima et al. have developed new void-free structures which use the poly-Si and crystal-Si bonding technique[4]. However these new structures have the high fabrication cost, because the fabrication process includes poly-Si deposition and its polishing.

In this paper, we propose a new SOI structure fabricated by a wafer direct bonding technique, which enable us to obtain low-cost intelligent power ICs.

2. New SOI Structure

Figure 1 shows a schematic cross-sectional view of the new SOI structure named partially bonded (PB) structure. In the PB structure, the gaps are fabricated under buried oxide films. The flow of the fabrication process is shown in Figure 2. (1)First, oxide films are formed on an N^- type Si substrate. (2)The oxide films are etched by HF solution until flat recesses of about 0.1 μm in depth are formed. (3)The wafer having the recesses and an N^+ wafer are treated with SC1 solution to remove particles from their bonding surfaces. In this process natural oxide films on the both wafers may facilitate bonding, we bonded these wafers without removing the natural oxide film. The surface having the recesses and N^+ substrate surface are bonded at room temperature. Then the bonded substrate is annealed in order to strengthen the wafer bonding. As a result, the gaps are formed between a buried oxide and an N^+ substrate. (4)The N^- substrate is ground and polished to form an active layer. The thickness of the active layer was determined by the breakdown voltage between source and drain of the VDMOS.

We fabricated the PB wafers by the above-mentioned process. As a starting materials, 125 mm (100) Czochralski silicon wafers were chosen with a resistivity of 1 Ωcm (phosphorus-doped) and 0.01-0.02 Ωcm (antimony-doped) for N^- and N^+ wafers, respectively. The heat treatment for the bonding is carried out at 1100℃ for 2 hours. The typical size of the buried oxide film is about 1 x 2 mm rectangle. The thickness of the buried oxide film is selected to be about 1 μm. After the bonding, the N^- substrate was ground and polished until its thickness became about 15-20 μm. Some PB wafers were annealed at 1200℃ for 15 hours. This heat treatment is equivalent to that in the full device fabrication process of the power ICs.

3 .Experimental Results and Discussion

3-1 Structure and voids

A void-free bonded interface at the VDMOS region of the PB structure is needed so that the drain current of the VDMOS flows vertically through the bonded interface. Voids on the bonding interface of the PB structure is observed by scanning acoustic tomography (SAT, Hitachi ST-100). Figure 3 shows a SAT image of the PB wafer after the bonding heat treatment. The white contrast in this image shows void generation. No void is observed at the VDMOS region; however, voids are partially observed at control circuit region. Figure 4 shows a cross-sectional SEM micrograph of the PB wafer. As shown in this picture, a gap is present under the buried oxide film in the PB wafer. Since the first bonding surfaces are mirror polished crystalline silicon surfaces and the buried oxide films and the N^+ substrate are not bonded, a void-free bonded interface was obtained at the VDMOS region. These results show that the crystallographically perfect bonding at VDMOS region has been achieved by the PB structure.

Figure 5 shows a SAT image of the PB wafer after the heat treatment (1200℃, 15 h). No void is observed at the VDMOS region; moreover, voids are observed only at the edge region of the control circuit.

Figure 6 shows a cross-sectional TEM image at the center of the control circuit region in the PB wafer after the heat treatment (1200℃, 15 h). As shown in this picture, no gap is observed under the buried oxide film at the center of control circuit region.

3-2 Crystalline defects

We have investigated crystalline defects in the PB wafers after the bonding heat treatment or the heat treatment (1200℃, 15 h). Figure 7, 8 indicate optical micrographs of the Wright etched active layer surface and cleavage surface of the PB wafer after the bonding heat treatment. These photos show no crystalline defect on these surfaces. Furthermore, no crystalline defect is observed on the Wright etched active layer surface and cleavage surface of the PB wafer after the heat treatment (1200℃, 15 h). Moreover, no crystalline defect was observed near the bonded interface in the PB wafers by cross-sectional TEM.

3-3 Electrical bonding

We also studied the electrical characteristics of the PB structure. Figure 9 shows the resistivity profile of the VDMOS region after the heat treatment (1200℃, 15 h) by means of spreading resistance technique. The profiles indicate that the no high resistivity region is present near the bonded interfaces.

4. Conclusion

A fabrication method of novel SOI structure by A wafer direct bonding technique has been developed and we have achieved crystallographically and electrically perfect bonding at the VDMOS region. Thus low cost intelligent power ICs will be fabricated by the present partially bonded SOI structure.

Acknowledgment

The authors would like to thank Sumitomo Sitix Corporation for the bonded wafer fabrication.

Reference

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[3] T.Ohoka et al. : Proc. ISPSD'93, (1993) 119.
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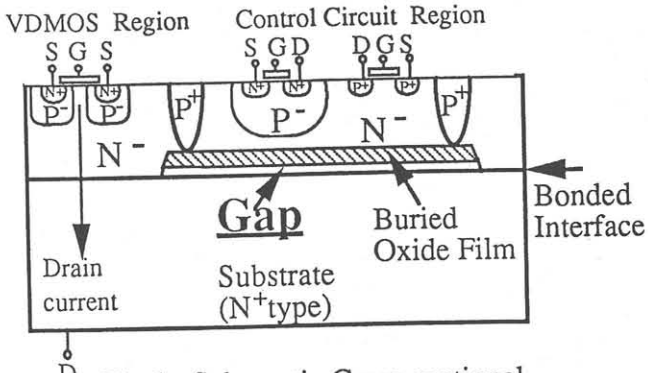

Fig.1. Schematic Cross-sectional View of the New Structure

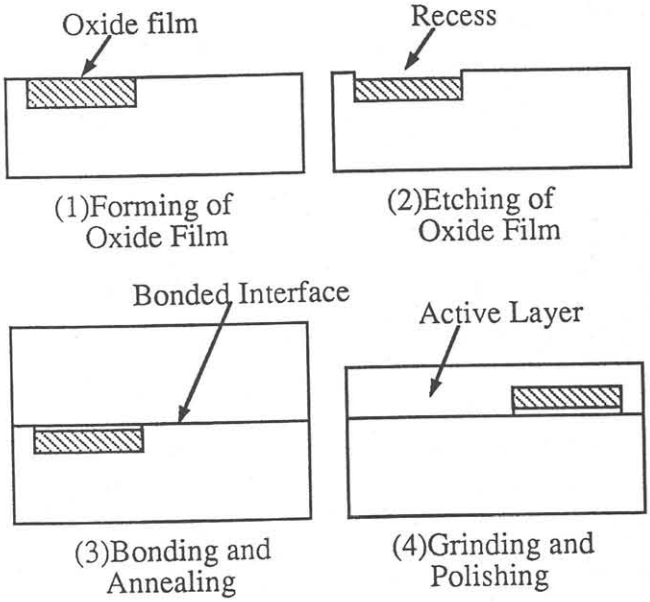

Fig.2. Fabrication Process of the New Structure

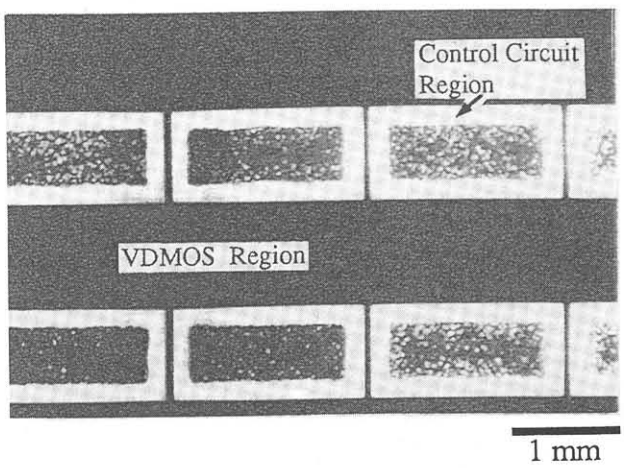

Fig.3 SAT Image of PB Structure after Bonding Heat Treatment

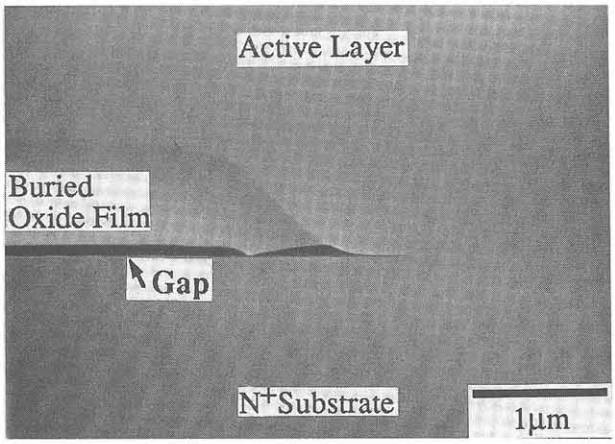

Fig.4 Cross-sectional View of PB Structure by SEM

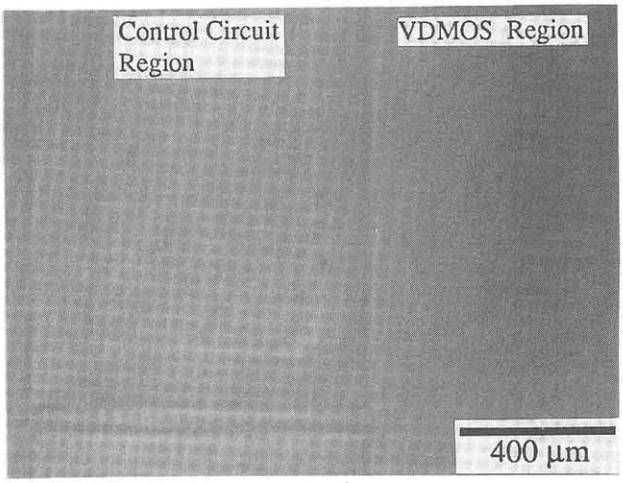

Fig.7 Plan View of the PB Structure by Optical Micrograph after Wright etching

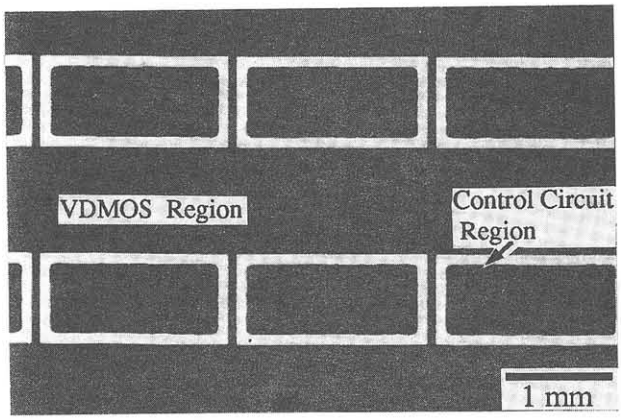

Fig.5 SAT Image of PB Structure after the Heat Treatment (1200℃, 15H)

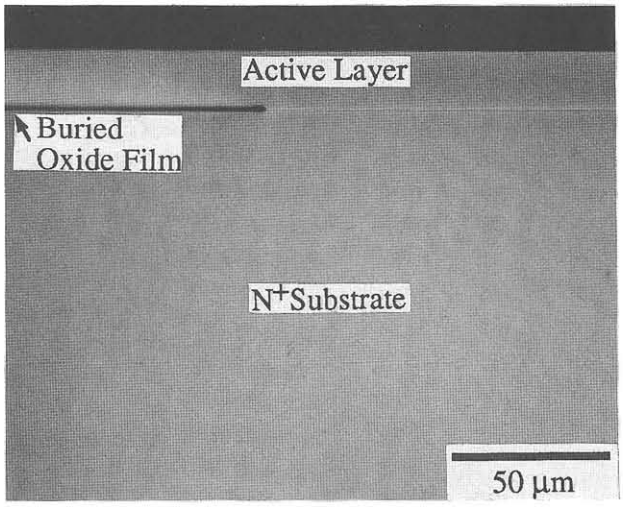

Fig.8 Cross-sectional View of the PB Structure by Optical Micrograph after Wright etching

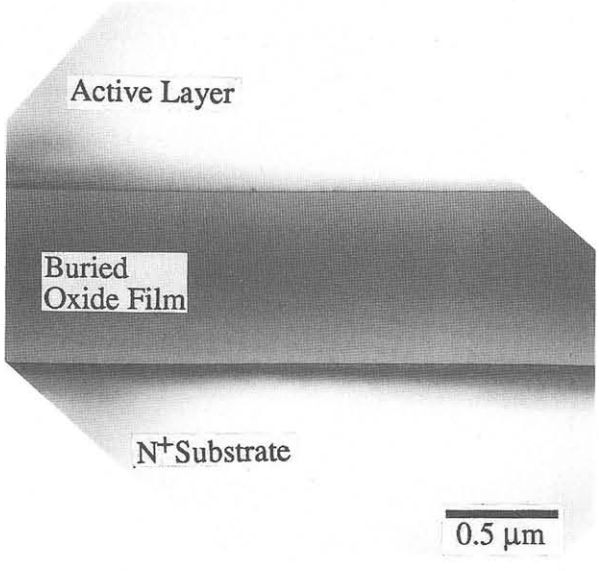

Fig.6 Cross-sectional View at the Center of Control Circuit Region by TEM

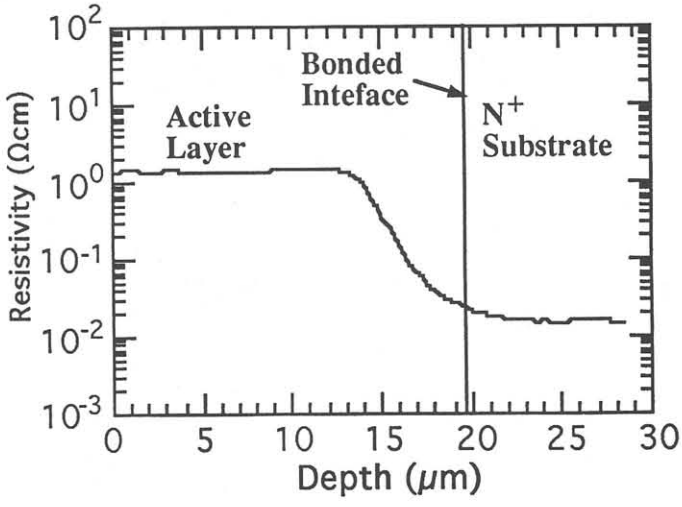

Fig.9 Resistivity Profile of the VDMOS region of PB Structure