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SOI LIGBT Structure with the Collector-Short Region for Improved Latch-Up Performance

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This paper describes the collector-short technique to improve the latch-up performance without the increase in the on-state voltage for the lateral insulated gate bipolar transistor (LIGBT) on the silicon-on-insulator film. The collector-short region is introduced in only the collector region at the sharp corner of the emitter region, where the minority carrier, which induces the latch-up, concentrates. The 1.5 times higher latching current in the static mode is accomplished without the deterioration of the on-state characteristic in comparison with the LIGBT without the collector-short region.

1. Introduction

The dielectric isolation technique using a silicon-on-insulator (SOI) film is a promising technology for high-voltage power ICs due to its superior isolation performance. The intelligent power ICs using this technique have already been developed[1]. The lateral insulated gate bipolar transistor (LIGBT) has become very attractive for use in output stage for the power ICs on the SOI film, due to its good performances[2]. Unfortunately, the LIGBT structure contains an inherent thyristor which can causes the device to latch-up, resulting in loss of the gate control. Especially, the latching problem in the LIGBT on the SOI film becomes worse than the equivalent device on the junction isolated wafer[3], because the substrate is no longer able to collect some of the minority carrier and device temperature increases significantly due to its high thermal isolation. Extensive attempts have been made to improve the latch-up performance in the LIGBT on the SOI film[4,5]. However, the improved latch-up performance can be obtained at the expense of an increase in the on-state voltage.

This paper reports the collector-short technique to improve the latch-up performance without the increase in the on-state voltage. The collector-short region is introduced in only the collector region at the sharp corner of the emitter region, where the minority carrier, which induces the latch-up, concentrates. The experimental results on the static latch-up current at room temperature is shown in comparison with that of the LIGBT without the collector-short region.

2. Device Description

Figure 1 shows the structure of the LIGBT on the SOI film. In Fig.1 Rb is the resistance of the p-base layer underneath the n^+-source layer and Ih indicates the current by the minority carrier, that is the hole current. The LIGBT contains the parasitic thyristor formed by n^+-source, p-base, n-drift and p^+-collector layers. When the voltage drop by Rb x Ih is sufficient to forward-bias the junction between the n^+-source and p-base layers, electron current (I_{Latch}) flows through this junction and the LIGBT loses the gate control. This is the latch-up phenomenon.

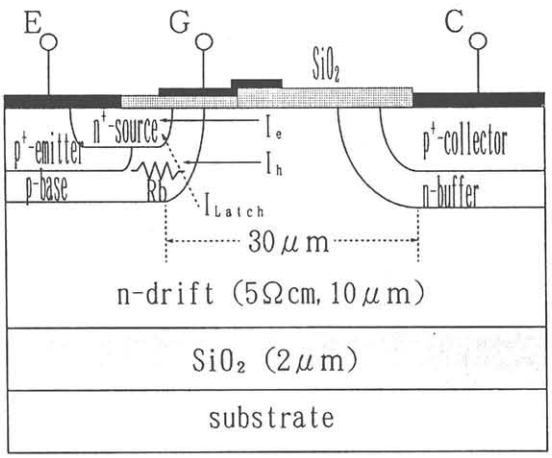

Fig.1 Cross sectional view of the fabricated LIGBT on the SOI film

Figure 2 illustrates the cell design of the LIGBT. As shown in Fig.2, the zigzag pattern like the teeth of a comb is normally adopted to the cell design for the LIGBT. This cell design comprises the linear and rounded parts. The rounded parts contain the emitter and collector corners. At the emitter corner, the emitter region has the sharp edge surrounding the collector region, so that the holes injected from the p^+-collector layer concentrate at the emitter region, as shown in Fig.3. Therefore, this corner is most susceptible to the latch-up. In this study, the n^+-collector-short layer is formed in the collector region at the emitter corner in order to prevent the injection of the holes, as shown in Fig.4. The surface structures corresponding to the emitter corner and other parts are illustrated in Fig.5. By replacing the p^+-collector layer at the emitter corner with the n^+-collector-short layer, the LIGBT includes the lateral MOSFET structure partially.

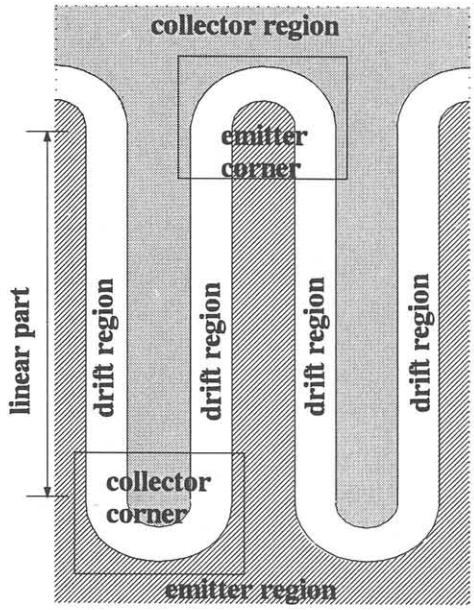

Fig.2 Top view of the LIGBT cell design

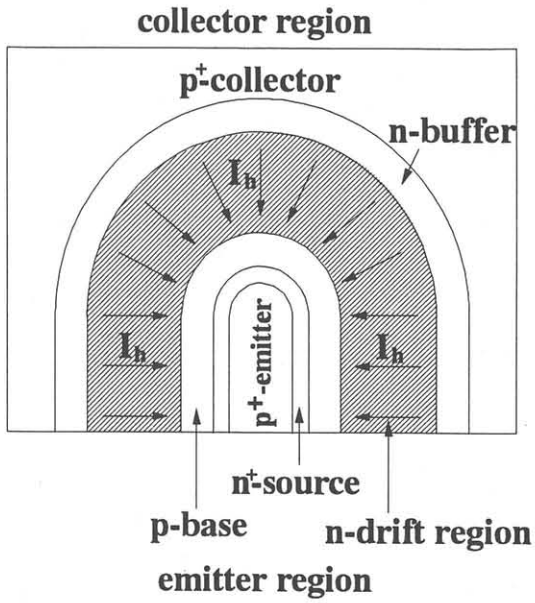

Fig.3 Hole current (I_h) flow path at the emitter corner

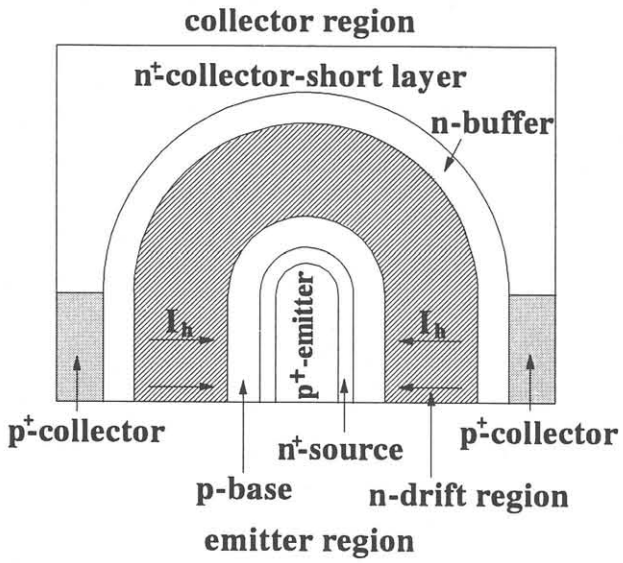

Fig.4 Hole current (I_h) flow path at the emitter corner with the n^+-collector-short layer

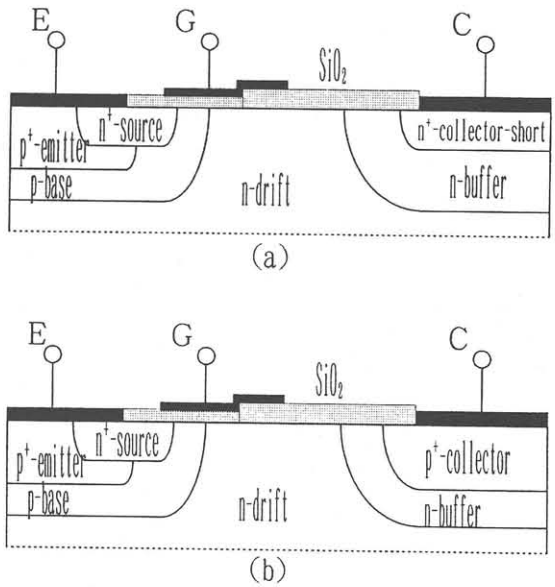

Fig.5 Surface structure of the LIGBTs (a) with and (b) without the n^+-collector-short layer

3. Experiment

Figure 1 also indicates the design of the fabricated devices. The conventional LIGBTs with and without the n^+-collector-short layer at the emitter corner were fabricated on the 10μm-thick SOI film with 2μm-thick bottom oxide, using the same wafer process for each. The n^+-collector-short layer was formed by the same implantation for the n^+-source layer. Fabricated LIGBTs had the drift length of 30μm, the channel length of about 2μm and the device size of 0.0022cm^2. The gate oxide thickness was 0.1μm. The threshold voltage, which is defined as the gate voltage at the collector current of 1μA, was about 1.5V. The breakdown voltages for both LIGBTs were more than 280V, as shown in Fig.6. In the cell design of the fabricated LIGBTs the length of the linear part was 1000μm, and the radius of the emitter and collector regions at the emitter corner were 11μm and 41μm, respectively. The fabricated devices contain two cells. The on-state voltage at 100A/cm^2 and the static latch-up current at room temperature of both LIGBTs were compared in this experiment.

Figure 7 shows the I-V waveforms at the gate voltage of 10V for both LIGBTs. The latch-up current of the LIGBT

with the collector-short region is 310A/cm^2, which is 1.5 times higher than that of the LIGBT without the collector-short region, nevertheless there is no difference of the on-state voltage, 1.8V at the current of 220mA (100A/cm^2) with the gate bias of 10V, between both LIGBTs. Experimental results show that the latch-up current can be increased without the increase in the on-state voltage.

4. Conclusion

The collector-short technique to improve the latch-up performance without the increase in the on-state voltage for the LIGBT on the SOI film is presented in this paper. The collector-short region is introduced in only the collector region at the sharp corner of the emitter region. The on-state voltage and the static latch-up current at room temperature of the LIGBTs with and without the n^+-collector-short layer were compared. The improved latch-up performance can be obtained without the deterioration of the on-state characteristic.

References

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2) Tomoko Matsudai et al, Proc. ISPSD, pp.399-403, 1994.
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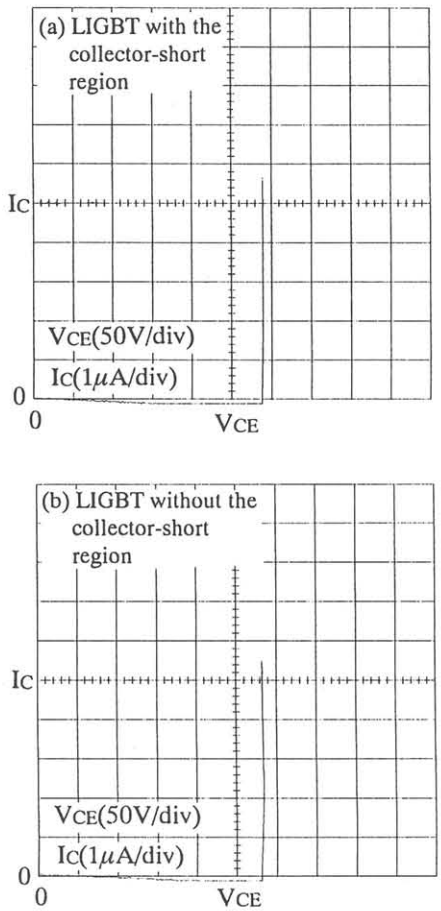

Fig.6 Measured breakdown characteristics

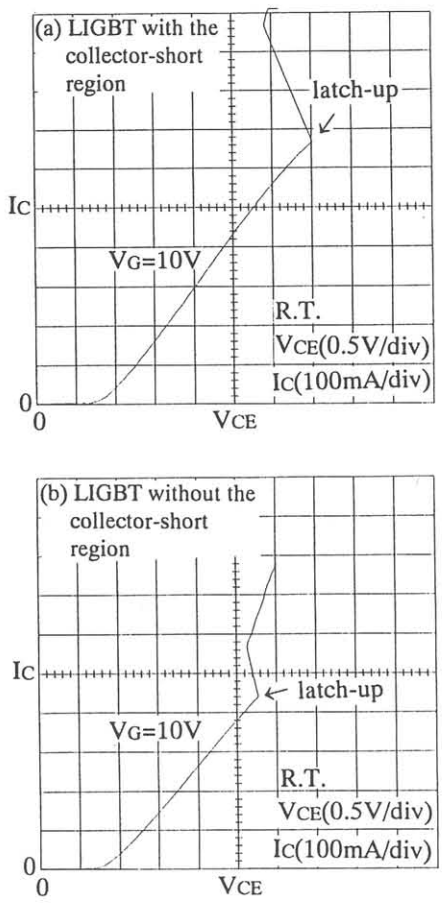

Fig.7 Measured I-V waveforms at the gate voltage of 10V