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Advantages of Ultra-Thin SIMOX/CMOS Based on Well-Established 0.8μm Mass-Production Technologies for Low Power 1V PLL Circuits

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This paper describes the various advantages of SOI circuits when well-established 0.8μm CMOS mass-production technologies for ultra-low power 1V PLL (Phase Locked Loop) are applied. From experiments on circuit operation, a parasitic capacitance of SOI is estimated about 80% of that of bulk, and it is found that the most advantage of SOI to bulk is 180% higher speed operation at low supply voltage due to less drain capacitance and less short channel effects of pMOSFET.

1. INTRODUCTION

Advantages of ultra-thin SOI structure compared with bulk structure, especially reduction of parasitic capacitance and suppression of short channel effects, are very attractive for low-power, low-voltage and high-speed CMOS applications. But there are few studies that the respective advantages are estimated from experiments on circuit operation quantitatively. Because exact comparison between SOI and bulk structure is very difficult due to differences of the device characteristics. For instance, a difference of delay times between the two structures with different threshold voltage is not caused from only parasitic capacitance but the device characteristics. This paper describes the method to analyze the circuit performances involving the different device characteristics and results of the analysis for the first time.

2. THEORY

In a CMOS inverter, charge current *ich*, discharge current *idc* and short circuit current *isc* flow as shown in Fig.1 if leakage current is negligible, where *Cp* is parasitic capacitance of the circuit.

From the fact that the components of currents determine the circuit performance such as speed and power dissipation, *Cp* should be estimated from both speed and power dissipation.

Supply current per operating frequency *Idd/f*, which means power dissipation per a cycle, comes from the following equation:

$$Idd/f = \int (ich+isc)\,dt = Cp\,Vdd + \int isc\,dt \quad \text{- - - (1)}$$

where *Vdd* is supply voltage. The first term is constant, but the second term varies as a function of drain current, threshold voltage of MOSFETs or operating frequency as shown in Fig.2. Therefore *Cp* and *isc* are available using dependence of *Idd/f* on the device characteristics such as *Vth* or *f*.

Delay time of a CMOS gate, caused by charge and discharge for the parasitic capacitance, depends on the capacitance and current drivability as:

$$Tpd = K\,Cp\,Vdd/\Sigma Ids \quad \text{- - - (2)}$$

where *Tpd* is the delay time, *K* is a constant related with threshold voltage of the CMOS gate and ΣIds is the total current dirvability of both channel of MOSFETs.

In the case of such ideal switching that no short circuit current flows in the circuit, ΣIds is calculated from:

$$\Sigma Ids = Idsn\,Idsp\,/(Idsn+Idsp) \quad \text{- - - (3)}$$

where *Idsn* and *Idsp* are drain currents of n-channel and p-channel MOSFETs respectively.

So *Cp* can be estimated from equ.2 and equ.3.

However, no information as to the circuit will be gotten from the equ.3 except estimation of *Cp*, and the equ.3 may not applicable when the short circuit current isn't negligible. So using unknown function $f(\alpha)$, we determine a new ΣIds as:

$$\Sigma Ids = (Idsn+Idsp)\,f(\alpha) \quad \text{- - - (4)}$$

where $\alpha = Idsp/Idsn$ - - - (5)

and in the ideal case from equ.3, $f(\alpha)$ can be shown as follows.

$$f(\alpha) = 1/(2+\alpha+1/\alpha) \quad \text{- - - (6)}$$

By using a plot of $f/(Idsn+Idsp)$ vs. α, it become possible to analyze speed characteristics of the circuit even if the circuit is not applicable to the ideal case described in equ.6.

3. FABRICATION AND MEASUREMENT

Using Separation-by-IMplanted-OXygen (SIMOX) wafers, SOI CMOS circuits are fabricated on the same process as well-established 0.8 μ m mass-production technologies. And bulk CMOS circuits are also fabricated using common layout masks for the

comparison of circuit performances with SOI. Key process and device parameters are listed in Table 1. On several wafers with different channel impurity dopings (Boron), 27-stage ring oscillators are tested at *1.0V* of supply voltage and the device characteristics of both MOSFETs corresponding to the ring oscillators are measured at *1.0V* of drain voltage respectively.

4. DEVICE CHARACTERISTICS

First, an estimation of *Cp* can be done from the viewpoint of the power dissipation of ring oscillators, where oscillating frequency *fosc=1/(54Tpd)*. Fig.3 shows supply current per oscillating frequency *Idd/fosc* versus oscillating frequency. It is considered that *isc* is negligible because clear slope is not observed. Thus *Cp* of SOI is estimated to be about 80% of that of bulk from equ.1.

Next, in order to discuss on the speed performance of the circuits, *fosc/(Idsn+Idsp)* versus α are shown in fig.4. Because the measured points at the same device structure but different *Idsn* and *Idsp* are roughly on the ideal curves, *isc* is also negligible, and *Cp* of SOI is estimated to be about 80% of that of bulk from equ.2 and equ.3.

Using the theoretical equations on *Idd/fosc* and *fosc/* Σ *Ids*, it is found that *Cp* of SOI can be estimated quantitatively from the investigation of ring oscillators for the first time. These results agree with each other and our simulated result[1] that *Cp* of SOI is estimated to be 85% of bulk and this difference is due to the reduced drain capacitance of SOI.

Fig.4 gives us an important information regarding operation of the CMOS circuits. When the ratio α is more than *0.5*, *fosc/(Idsn+Idsp)* is almost constant (less than 10% of a fall from the maximum at $\alpha=1$). But it decreases rapidly and approaches to zero as α becomes less than *0.5*. However α is less than *0.5* ordinarily due to lower mobility and worse short channel effect of pMOSFETs than nMOSFETs because pMOSFETs are buried channel type.

It is confirmed that short channel effect of SOI-pMOSFET is better than that of bulk as shown in Fig.5, where *S* factor is a swing of sub-threshold curve, *Leff* is an effective channel length. Thus SOI-pMOSFET has more Idsp than bulk if the threshold voltages are controlled on the same level of leakage current as bulk. Regarding nMOSFETs, clear differences between SOI and bulk are not found in short channel effects.

If the leakage currents of circuits are in the same level with reduced *Vth* of SOI-pMOSFET, the SOI circuit can operate faster than the bulk circuit because SOI devices have more *Idsn+Idsp* and *fosc/(Idsn+Idsp)* due to lager α and less *Cp* than bulk. For example, the SOI circuit is 80% faster than bulk, keeping leakage current below $0.1nA/\mu m$. (In this case, α of bulk is only *0.23* but α of SOI is *0.35*.)

In the other approach, if SOI circuit speed is decreased to a bulk level by increasing *Vth*, more than a decade of leakage current decrease in comparison with bulk, and supply current becomes less than 80% of bulk because decrease of *isc* can be expected.

5. DEMONSTRATIONS

In order to confirm the above SOI circuit performances, PLL ICs, which contain dual modulus prescaler divided by 64/65, are demonstrated. Fig.6 shows supply current versus operation frequency of two SOI PLLs and a bulk PLL at *1V* of supply voltage. SOI-A, in the same leakage level as bulk, can operate at the fastest frequency of *340MHz* (190% of bulk). Such a high performance cannot be realized for bulk even if *Vth*'s are more reduced at *1V* of supply voltage. And SOI-B, in the same maximum frequency they can operate as bulk, consumes the least current of *0.49mA* (75% of bulk) at *fin=100MHz*.

6. CONCLUSION

We have demonstrated high performances, especially high-speed operation at reduced supply voltage, of ultra-thin SIMOX/CMOS circuits fabricated by well-established 0.8 μ m CMOS mass-production technologies, leading to commercially available 1V PLL. The performances are realized by their essential advantages such as reduced parasitic capacitance and suppression of short channel effects which are estimated quantitatively in this paper.

It can be expected that drastic low-power dissipation is available when supply voltage is reduced lower than conventional circuits by making the best use of the high-speed characteristics of SOI.

REFERENCE

1) S.Warashina et al,"Scaling Merits of Ultra Thin Film SOI/CMOSFET's for Low Power Dissipation", SSDM'94, pp.298-300

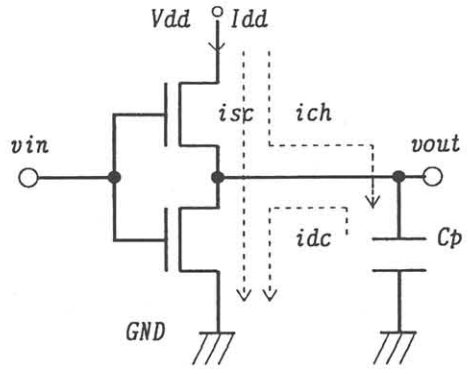

Fig.1 Currents in a CMOS inverter

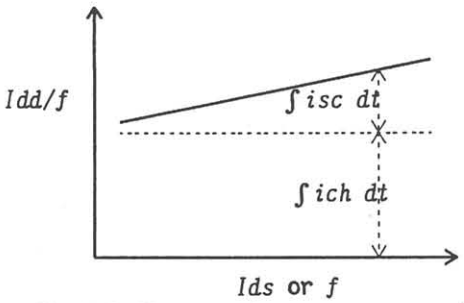

Fig.2 Influence of a *isc* component

Table 1 Process and device parameters

SOI thickness	:	100nm
Buried oxide	:	400nm
Gate oxide	:	15nm
Gate electrode	:	P-diffused poly-Si
Gate length	:	0.8 μm
Device width	:	16 μm (nMOS and pMOS)
Drain structure	:	single drain
Vth	:	$\pm$0.1~0.5V

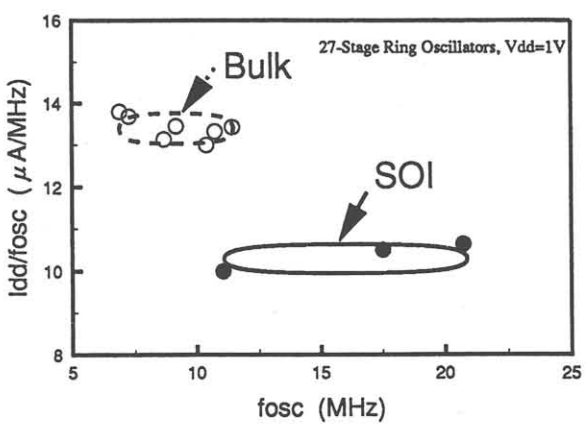

Fig.3 Normalized Power Dissipations

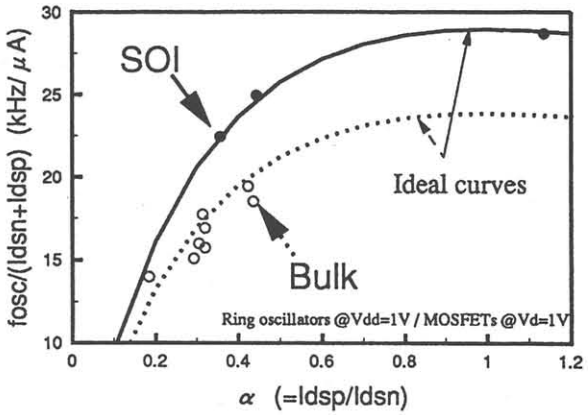

Fig.4 Analysis on Speed and Current Drivabilities

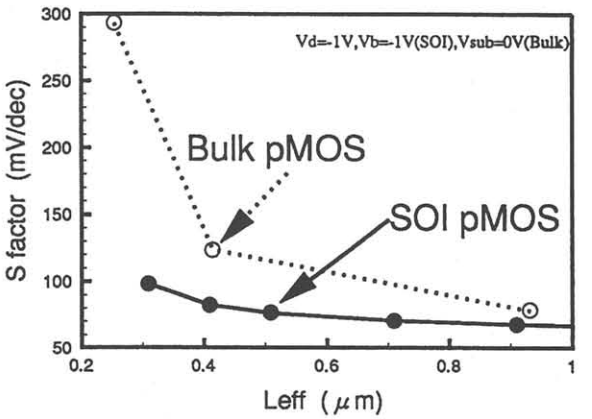

Fig.5 Short channel effects of pMOSFETs

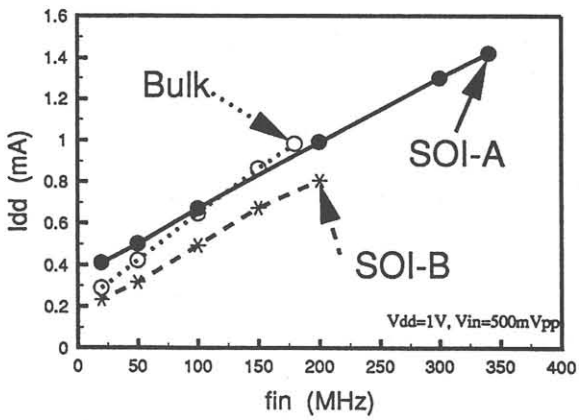

Fig.6 Operating characteristics of PLLs