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Analysis of Si-Ge Source Structure in 0.15 μm SOI MOSFETs Using Two-Dimensional Device Simulation

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This paper describes the technological potential of the bandgap engineering technique using a Si-Ge source structure in SOI MOSFETs. The detailed mechanism as well as the structure dependence for suppression of the floating-body effect in 0.15 μm gate-length SOI MOSFETs have been studied using a two-dimensional simulation. It has been found that the BVds improvement is strongly dependent on the lateral position of the Si-Ge layer to the source-to-channel p-n junction. It has also been predicted that the encroachment of the Si-Ge layer into the channel region is effective to achieve the maximum BVds improvement. The BVds improvement has been predicted to reach 1.5 V if it is possible to lower the energy barrier at the p-n junction in case where ΔEg = 0.2 eV.

1. INTRODUCTION

Silicon-on-insulator (SOI) devices are expected to offer great potential for realizing low-power and high-speed ULSIs, which are essential for portable, multimedia computer systems. In applying SOI devices to practical ULSIs, however, the critical drawback is the floating-body effect, which causes a lowering of the drain-to-source breakdown voltage (BVds) [1], the appearance of kinks in the Id-Vds characteristic [2], anomalous subthreshold swings, and Vth shifts [3]. To suppress these effects, we have proposed and experimentally demonstrated the bandgap engineering technique, in which a narrow bandgap material, $Si_{1-x}Ge_x$, is formed using Ge implantation in the source region [4][5]. The aim of this technique is to remove the excess holes in the channel region by forming a heterojunction near the source / channel interface.

In this work, we investigate the technological potential of the bandgap engineering technique of using the Si-Ge source structure. The detailed mechanism as well as the structure dependence of BVds improvement in 0.15 μm gate-length SOI MOSFETs is studied using a two-dimensional simulation. It has been found that the BVds improvement is strongly dependent on the lateral position of the Si-Ge layer. It has also been clarified that bandgap engineering in the proximity of the source-to-channel p-n junction is important to realize the maximum performance.

2. SIMULATION

Figure 1 shows a cross section of the n-type thin-film SOI MOSFET used in this analysis. Here, n^+-regions and the channel region were approximated to have rectangular shape. The Si-Ge region was also assumed to be rectangular. The Ge ratio x in the $Si_{1-x}Ge_x$ was in most cases equal to 0.1, which was shown to correspond to a bandgap narrowing of approximately 0.1 eV [1], except in cases where the bandgap narrowing dependence of BVds improvement was investigated. In ignoring the effect of the Si-Ge layer on impact ionization near the drain region, the Si-Ge layer is only formed on the source region. The device structure was optimized in terms of the short channel effect at 0.15 μm gate length : W / L = 0.15 μm / 0.15 μm ; T_{SOI} = 30 nm ; the impurity concentration in the channel region and that in the source / drain n^+-region was 8×17 cm^{-3} and 1×20 cm^{-3}, respectively. Under these conditions, the SOI MOSFETs were of the fully-depleted type. A two-dimensional device simulator (MOS2C), in which physical parameters such as bandgap, mobility, impact-ionization rate, etc., were modified to deal with the Si-Ge structure, was used.

Figure 2 shows a comparison of Id-Vds curves for SOI MOSFETs with and without a Si-Ge source. Here, a Si-Ge layer was formed on the source and drain regions to enable comparison of Id-Vds characteristics between experiment and simulation. It can be seen that the drain breakdown voltage improvement (ΔBVds) by using a Si-Ge

structure is reproduced. Hereinafter, ΔBVds is defined at Id = 0.1 mA, Vgt = 0 V (Vgt = Vg – Vth). In the simulated structure shown in Fig. 2 (b), ΔBVds was 0.9 V, which was close to the value obtained in the experiment.

3. RESULTS and DISCUSSION

It has been found that the BVds improvement tends to saturate as the Ge content ratio x is increased, as shown in Fig. 3. This is attributed to a tendency of hole flow to saturate with bandgap narrowing, i.e., the hole current enhancement becomes smaller as the valence band shift becomes larger. This is because the energy barrier for holes at the p-n junction tends to limit hole current for a valence band shift larger than 0.2 eV. Nevertheless, it should be noted that a Ge ratio as small as 0.1 can realize an approximately 1 V improvement in BVds.

Figure 4 shows that as the Si-Ge layer thickness increases, ΔBVds also increases. This can be explained by an increase in hole-current "conductance" as the Si-Ge layer is made thicker. However, it can be seen that even a 10 nm Si-Ge layer (T_{SiGe} / T_{SOI} = 33 %) realizes approximately 80 % of ΔBVds which is achieved by a 30 nm-thick Si-Ge layer. In Fig. 4, the Si-Ge layer thickness is increased from the buried-oxide side to the gate-oxide side. Still, the same tendency has been obtained for the case of increasing the Si-Ge layer thickness to the contrary. Figure 5 demonstrates how holes are absorbed by the Si-Ge layer which is partially formed in the source region.

The lateral spacing between the Si-Ge layer edge and the metallurgical p-n junction, x, influences ΔBVds significantly, as shown in Fig. 6. As the edge of Si-Ge layer approaches the p-n junction ($\Delta x < 0$ nm), ΔBVds increases abruptly. It should be noted that, as the Si-Ge edge further moves into the channel region ($0 \text{ nm} \leq \Delta x$), ΔBVds continues to increase and reaches a maximum (at $\Delta x = 10$ nm for 0.1 Ge content). When the Si-Ge edge further encroaches into the channel region, ΔBVds begins to decrease ($\Delta x > 10$ nm). These phenomena are explained in Fig. 7, where three cases of lateral position for the Si-Ge layer are shown, i.e., (A) $\Delta x < x_1$ (= 0 nm), (B) $0 \leq \Delta x \leq x_2$ ($\cong$ 10 nm), and (C) $\Delta x > x_2$. In case (A), the hole current increases as the Si-Ge edge approaches the p-n junction. Here, the Si-Ge layer is considered to increase the hole-current conductance from the channel to source regions because the intrinsic carrier density in Si-Ge (n_{ie}) is greater than that in Si (n_i) as follows.

$$n_{ie}^2 = n_i^2 \exp(\Delta Eg / kT)$$

Here, ΔEg is the amount of the valence band shift. As the Si-Ge layer approaches the channel region, the efficiency of excess hole absorption increases, resulting in a BVds increase. In case (B), the hole current increases because the energy barrier height for the hole-current is significantly reduced. In case (C), holes come to accumulate in an "energy dip", and the hole-current decreases because the energy barrier for holes rises again at the p-n junction boundary. It should be added in Fig.6 that the ΔEg dependence of ΔBVds in the case where the Si-Ge layer is inside the channel region is much larger than the case where the Si-Ge layer is in the source region.

These results indicate that it is possible to realize the greater potential of the bandgap engineering method if the Si-Ge layer can be placed in the channel region.

4. CONCLUSIONS

We have analyzed the mechanism and structure dependence of the bandgap engineering technique using a Si-Ge source structure in thin-film 0.15 μm SOI MOSFETs. The simulation revealed that using the Si-Ge formation which is self-aligned to the gate, ex. Ge implantation, an approximately 1 V improvement in BVds for 0.15 μm SOI MOSFETs can be expected at maximum for $\Delta Eg = 0.2$ eV. Furthermore, it was confirmed that BVds improvement can be further increased to 1.5 V if it is possible to reduce the energy barrier at the p-n junction by making the Si-Ge layer to encroach into the channel region.

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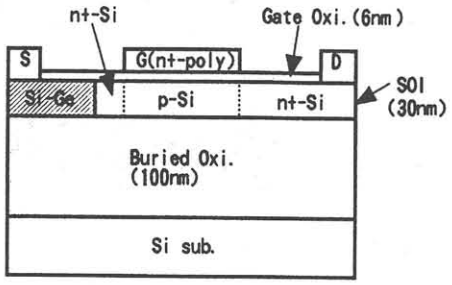


Fig.1 Cross section of SOI device structure for analysis.

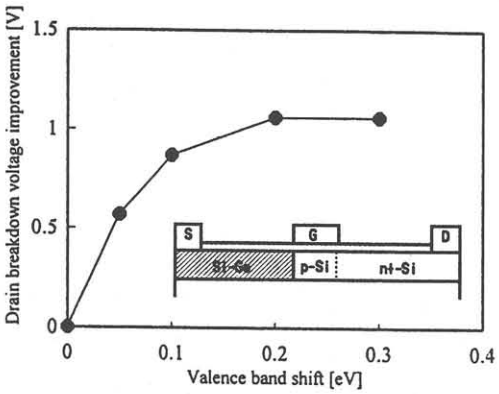


Fig.3 Valence band shift versus drain breakdown voltage improvement.

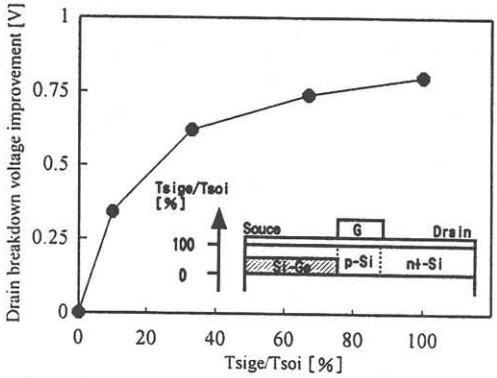


Fig.4 Si-Ge layer thickness versus drain breakdown voltage improvement.

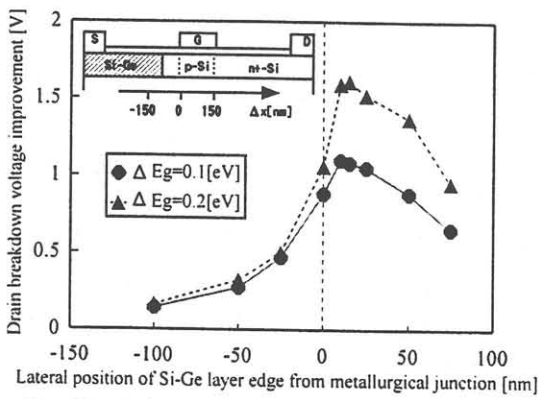
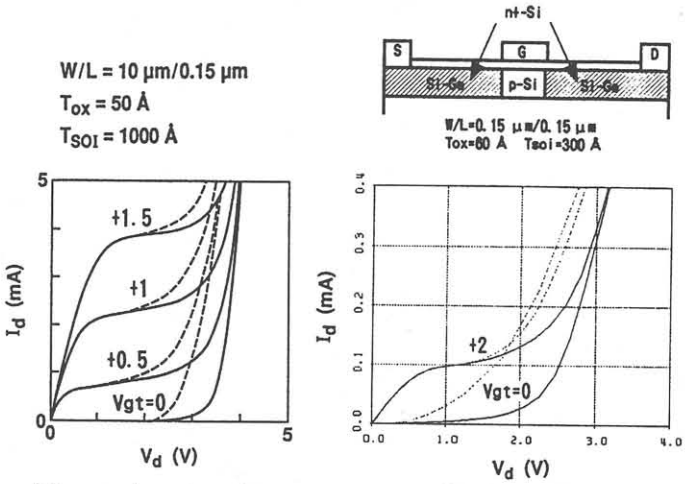


Fig.6 Drain breakdown voltage improvement as a function of lateral position of Si-Ge layer edge from metallurgical junction at source.



(a) experiment (ref.[1]) **(b) simulation**

Fig.2 Comparison of Id-Vd curves between SOI MOSFET with (solid lines) and without (dashed lines) Si-Ge source.

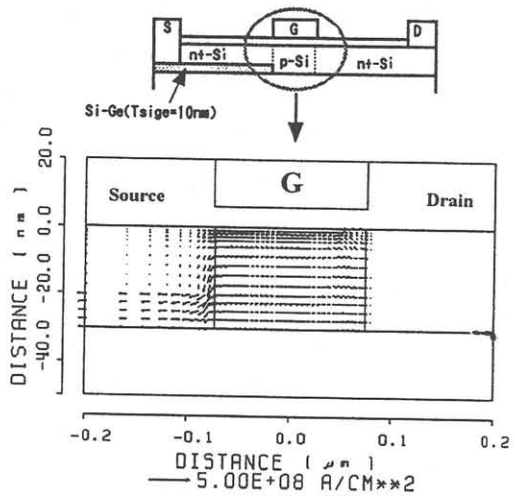


Fig.5 Typical hole current vector in Si-Ge source at Vgt = 0 V. Excess holes are absorbed into the 10 nm-thick Si-Ge layer.

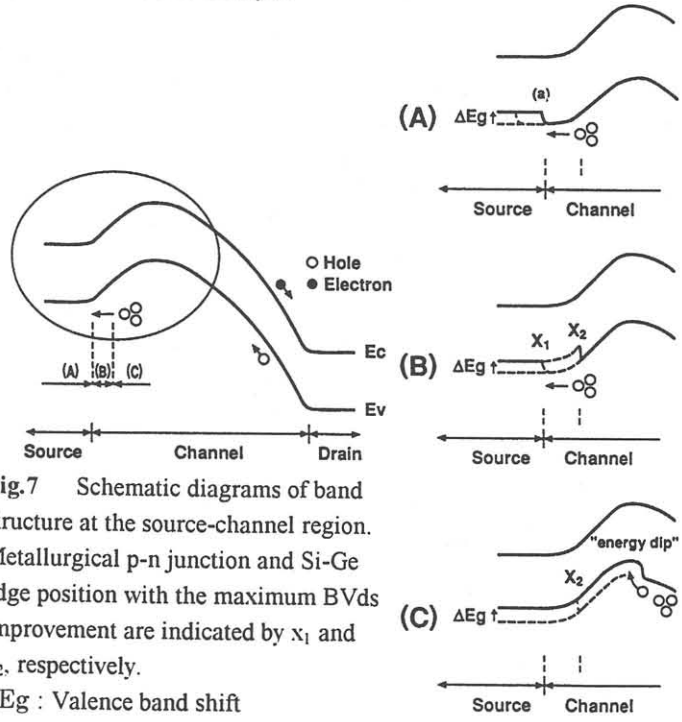


Fig.7 Schematic diagrams of band structure at the source-channel region. Metallurgical p-n junction and Si-Ge edge position with the maximum BVds improvement are indicated by x_1 and x_2, respectively.

ΔEg : Valence band shift