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Modeling on the Channel-To-S/D Capacitance and the Short Channel Effect for 0.1μm Fully Depleted SOI-MOSFET

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This paper proposes a simple analytical model on the short channel effect for the fully depleted SOI-MOSFET. The influence of the two dimensional effect is included based on the spatial distribution for the channel-to-S/D (source and drain) capacitance [1)2)] which is determined by an empirical expression. This treatment makes it possible to estimate the two dimensional effect without solving Poisson's equation which requires a large computation time. This model describes the short channel effect down to 0.1μm regime.

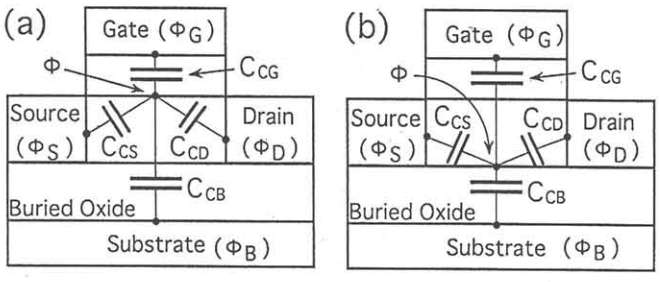

FIg.1 The capacitance net work model. (a) is for the surface conduction,(b) is for the back interface conduction

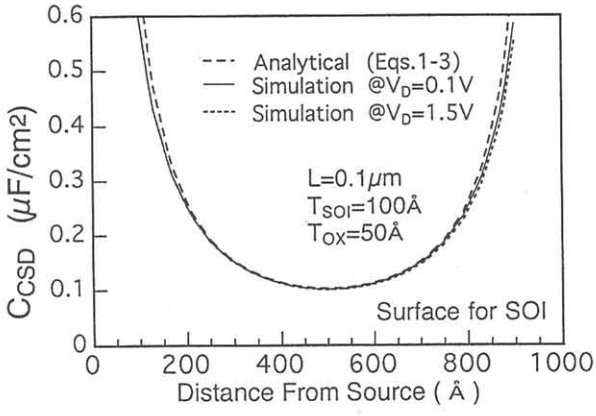

Fig.2 The horizontal distribution for C_{CSD} (the sum of C_{CS} and C_{CD}). Broken line shows the result given by Eqs.1-3. Solid line and dotted line show the simulation results.

1.Model Consider a capacitance network, which determines the potential for the fully depleted SOI-MOSFET, as shown in Fig.1. We propose empirical expressions which represent the channel-to-source capacitance C_{CS}, and the channel-to-drain capacitance C_{CD}, as in Eqs.1 and 2.

$$C_{CS}(x) = \frac{\alpha'\,(T_{SOI} + \beta')}{x^2 + \gamma' x}\,\varepsilon_0\,\varepsilon_{OX} \qquad (1)$$

$$C_{CD}(x) = \frac{\alpha'\,(T_{SOI} + \beta')}{(L-x)^2 + \gamma'(L-x)}\,\varepsilon_0\,\varepsilon_{OX} \qquad (2)$$

Where, T_{SOI} is the SOI thickness, x is the horizontal position (x = 0 for the source junction), L is the gate length, α', β' and γ' are fitting parameters whose values are 2.29, 70A and 50A, respectively. β' is a parameter which is introduced in order to include the influence of the electric field from the buried oxide. In Eqs.1 and 2, the dependence on the bias voltage and on the vertical position are neglected, since these dependencies are found to be small from device simulation.

C_{CSD} is determined as the sum of C_{CS} and C_{CD} as in Eq.3.

$$C_{CSD}(x) = C_{CS}(x) + C_{CD}(x) \qquad (3)$$

The horizontal distribution for C_{CSD} (Fig.2) and the dependence of C_{CSD} on the device structure (Fig.3) show excellent agreement with the numerical simulation results.

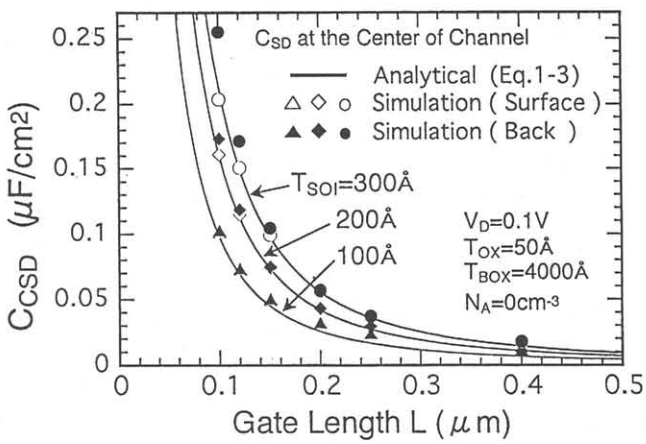

Fig.3 The C_{CSD} dependence on the device structure.

The potential in the SOI layer ϕ, threshold voltage V_{th} and subthreshold swing S are derived using C_{CS} and C_{CD} as follows. ϕ is given by Eq.4 by considering the capacitance network (Fig.1a and b),

$$\phi = \frac{C_{CG}\,\phi_G + C_{CS}(x)\,\phi_S + C_{CD}(x)\,\phi_D + C_{CB}\,\phi_B}{C_{CG} + C_{CS}(x) + C_{CD}(x) + C_{CB}} \qquad (4)$$

where, ϕ_S is the source potential, ϕ_D is the drain potential, ϕ_G is the gate potential and ϕ_B is the substrate potential.

C_{CG} is the channel-to-gate capacitance, which is given by Eqs.5 and 6.

$$C_{CG} = \varepsilon_0 \varepsilon_{OX} / T_{CG} \quad (5)$$
$$T_{CG} = T_{OX} + y\, \varepsilon_{OX} / \varepsilon_{Si} \quad (6)$$

Where, T_{OX} is the gate oxide thickness and y is the depth from SOI surface. In the following discussions, y corresponds to the distance between the SOI surface and the position where the subthreshold current flows. C_{CG} is assumed to be independent of horizontal position.

C_{CB} is the channel-to-substrate capacitance, and this capacitance is neglected in the following discussion since its value is small for the SOI-MOSFET.

Since V_{th} is the gate voltage which provides the inversion potential ϕ_{inv} in the SOI layer, V_{th} is derived from Eq.4 as in Eq.7 for the intrinsic SOI layer.

$$V_{th} = \frac{(C_{CG}+C_{CS}'+C_{CD}')\,\phi_{inv} - C_{CS}'\,\phi_S - C_{CD}'\,\phi_D}{C_{CG}} + \Phi_{ms} \quad (7)$$

Where, C_{CS}' and C_{CD}' represent C_{CS} and C_{CD} at the position where the potential is the minimum along the channel (potential barrier position). C_{CS}' and C_{CD}' are determined by substituting the potential barrier position , which is calculated using Eq.4 as shown in Fig.4, into x in Eqs.1 and 2. Φ_{ms} is the difference of the work function between the gate electrode and the source electrode.

The subthreshold swing S is given by replacing C_{CB} for the usual definition of the S factor(Eq.8), by the sum of C_{CS}' and C_{CD}' as Eq.9, since C_{CB} is small, and C_{CS}' and C_{CD}' are important for the short channel fully depleted SOI-MOSFET.

$$S = (kT/q)\ln(10)\,(1+C_{CB}/C_{CG}) \quad (8)$$
$$S = (kT/q)\ln(10)\,(1+(C_{CS}'+C_{CD}')/C_{CG}) \quad (9)$$

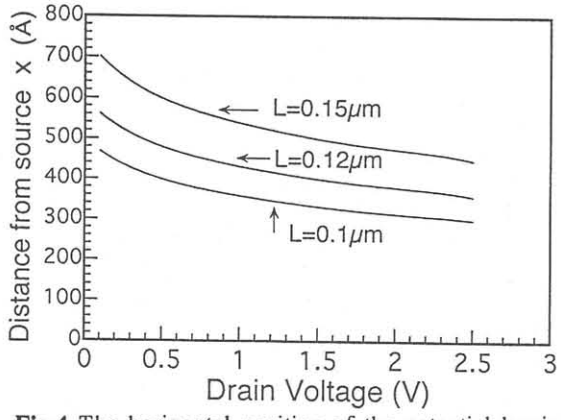

Fig.4 The horizontal position of the potential barrier which is calculated using Eq.4

2.Result The two dimensional potential distribution given by Eq.4 is shown in Fig.5. The S factor given by Eq.9 and V_{th} given by Eq.7 are shown in Fig.6. Their agreement with the numerical simulation indicates that the above model is valid to deal with the short channel effect for the fully depleted SOI-MOSFET.

For the low drain voltage, where the potential barrier is located near the center of the channel, S can be reduced to a very simple form as shown in Eq. 10.

$$S = (kT/q)\ln(10)\left(1 + \frac{\alpha T_{CG}(T_{SOI} + \beta)}{L^2 + \gamma L}\right) \quad (10)$$

$$T_{CG} = T_{OX} + d\, T_{SOI}\, \varepsilon_{OX} / \varepsilon_{Si} \quad (11)$$

where, α, β and γ are fitting parameters, whose value are 18.3, 70A and 100A, respectively. T_{CG} is the effective gate oxide thickness, which is given by Eq.11. where, d is a parameter for the back channel, whose value is zero for the surface channel, and unity for the back channel.

Equation 10 can provide a convenient way to estimate the S factor dependence on the device structure, as shown in Fig.7. Simulation results for intrinsic SOI body is inserted in Fig.7. The simulation results agree with the S factor for the back channel conduction.

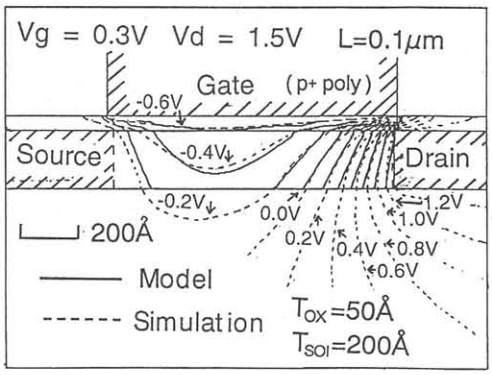

Fig.5 The potential distribution given by Eq.4. The depletion layer at the drain junction is determined as 20Å, and it is added for the gate length to correct the potential profile near drain. However this correction is neglected in the following discussion, since its influence is small for the potential barrier.

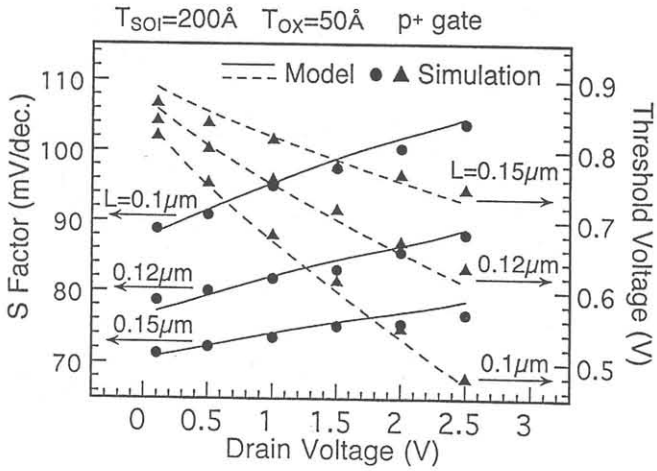

Fig.6 The dependence of S factor and V_{th} on the drain Voltage for L=0.1μm,0.12μm and 0.15μm. The floating body effect is neglected in the device simulation to distinguish the short channel effect.

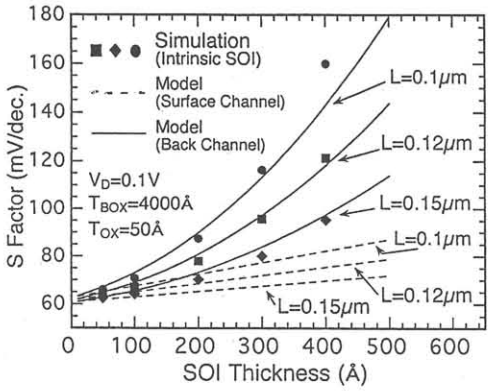

Fig.7 S factor dependence on the device structure for the SOI-MOSFET, which is given by Eq.10. The solid lines show the result for the back interface conduction, and broken lines for the surface conduction. Simulation is done for the intrinsic SOI.

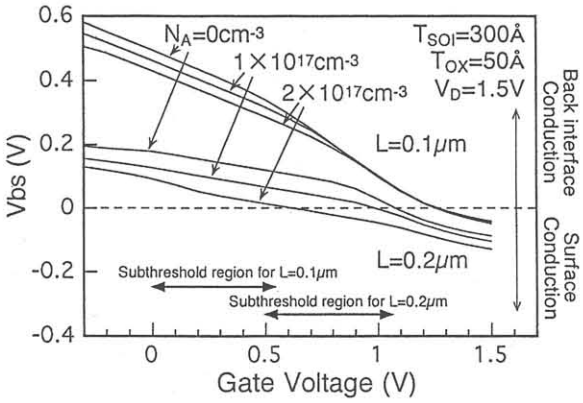

Fig.8 The dependence of the potential difference between the SOI back interface and the surface on the acceptor concentration. Positive value indicates that the back interface potential is larger than surface, and that the subthreshold current flows at the back interface.

3.Discussion on the back channel influence Equations 7,9 and 10 indicate that the short channel effect depends not only on C_{CS} and C_{CD} discussed above, but also on the depth of the channel in the SOI layer which determines T_{CG} and C_{CG}. Therefore, the condition for the back channel formation is investigated using device simulation. The potential difference between SOI back interface and surface (V_{bs}) is shown in Fig.8 for L=0.1 μm and 0.2 μm, where the positive value represent the case where the potential of back interface is larger than the surface. The increase in the back interface potential is caused by the electric field from the source and the drain. When V_{bs} is positive, the subthreshold current flows at the back interface where the gate controllability is worse, and the short channel effect is enhanced (T_{CG} increases in Eqs.5 and 10, C_{CG} decreases in Eqs.7-9).

For L=0.2 μm, V_{bs} becomes negative for higher accepter concentration at the subthreshold region, since the electric field from acceptor ions lower the back interface potential. However, it can not be negative for L=0.1 μm. One reason is that the channel-to-S/D capacitance increases drastically by reducing the gate length from 0.2 μm to 0.1 μm, as shown in Fig.3. This leads to a increase in V_{bs}. Another reason is that the static electrical coupling between the acceptor ions and the S/D electrode increases, and consequently the coupling between the acceptor ions and the gate electrode decreases, as the gate length decreases. This effect prevents the back interface from being lowered by the electric field from acceptor ions, then the V_{bs} dependence on the acceptor concentration becomes smaller for L=0.1 μm than for L=0.2 μm, as shown in Fig.8. The back channel formation can be discriminated by Eq.12, where V_{bs} is calculated from Eq.4 and ζ is a parameter less than unity that increases as the gate length decreases.

$$V_{bs} > (1-\zeta)\, qN_A T_{SOI}^2 / 2\,\varepsilon_{OX}\,\varepsilon_0 \qquad (12)$$

4.Device design for 0.1 μm SOI-MOSFET The above result indicates that a drastic increase in C_{CSD} (Fig.3) enhances the short channel effect for 0.1 μm SOI-MOSFET (Fig.7), and that the ultra thin SOI layer (< 200A) is efficient to eliminate this effect by compensating the increase in C_{CSD} (Fig.7 and Eqs.1-3), and by increasing the gate-to-channel capacitance when the back channel is formed (Fig.7 and Eqs.7,9,10), for the fully depleted SOI-MOSFET.

5.Conclusion It is shown that the V_{th} shift and the degradation of S factor due to the two dimensional effect, can be derived from a simple analytical model using empirical channel-to-S/D capacitance for the fully depleted SOI-MOSFET. This method does not require to solve the Poisson's equation. A simple formula that provides the S factor dependence on the gate length, SOI thickness and the gate oxide thickness for low drain bias, is also obtained based on the model. Device design for 0.1 μm SOI-MOSFET is discussed based on the above model. This model is valid for describing the short channel effect down to 0.1μm regime, where the two dimensional effect is significant even for the fully depleted SOI-MOSFET.

References

1) Koh.et.al Ext. Abs. 1994 SSDM (1994.Aug.), p.295
2) Koh.et.al IEICE Tech. Rep. **SDM94-207** (1995.Mar.), p.17, in Japanese .