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A 0.25μm CMOSFET Using Halo Implantation for 1Gb DRAM

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A 0.25μm CMOSFET has been developed using halo implantation for 1Gb DRAM. This technology features a source/drain implantation followed by a halo implantation with a tilted angle after formation of oxide side-wall spacer. The halo implantation is performed without additional implantation masks. Dopants formed by the halo implantation act as the punchthrough stopper that surrounds the LDD implantation region. As a result, the short channel effect of the halo MOSFET is drastically suppressed as compared with that of the conventional MOSFET and the Bvdss margin is remarkably improved more than 0.05μm for NMOS and 0.12μm for PMOS.

1. Introduction

The development of quarter micron CMOS devices requires drain engineering, which is one of the most important technologies in the quarter micron device since Vth roll-off characteristics and punchthrough due to short channel properties are serious problems for a deep submicron MOSFET[1]. These problems come from the widening of the depletion region and increasing of the drain electric field. Therefore, in order to solve the above problems, a wide variety of drain engineerings have been proposed[2)3)4)]. Recently, a halo implantation has been focused as one of the promising drain engineerings. It has been performed using additional implantation masks after LDD implantation[2)3)], or executed by complicated self-aligned manner[5]. In this paper, a 0.25μm CMOSFET utilizing a simple and cost-effective halo implantation for 1 Gb DRAM is discussed and compared with the conventional CMOSFET. The halo implantation is performed without additional implantation masks. Dopants formed by the halo implantation act as the punchthrough stopper that resists effectively the punchthrough from drain to source. The Vth roll-off characteristics of the halo MOSFET are drastically suppressed as compared with those of the conventional MOSFET. The Bvdss margin is remarkably improved more than 0.05μm for NMOS and 0.12μm for PMOS. Hence, a 0.25μm CMOSFET becomes practical for highly manufacturable 1 Gb DRAM.

2. Fabrication procedure

The process condition for a halo CMOSFET is summarized in Table I. and the process sequence of the halo implantation is illustrated schematically in Fig. 1. The major feature of this process for halo CMOSFET is that halo implantation is performed without additional implantation masks. Oxide side-wall spacer is formed after the blanket N-LDD implantation(Phos., 1.0E13, 30KeV). Then, the halo implantation is carried out with a tilted angle and the source/drain implantation is followed. These halo dopants have proper doping profile which effectively surrounds LDD region as shown in Fig. 1(c).

Table I. Process conditions for the halo CMOSFET.

Process step	NMOS	PMOS
Isolation	LOCOS	
Well	B,3.0E13,500KeV	P,3.0E13,800KeV
channel IIP	BF2,2.0E12,60KeV	BF2,5.5E12,60KeV
Gate Ox.	60A	
N-LDD IIP	P,1.0E13,30KeV Blanket	
Spacer	Oxide side-wall 500A	
Halo IIP	Skip(conventional)	
	B,6.0E12,30KeV,45° B,6.0E12,50KeV,45°	P,2.4E13,80KeV,30° P,2.4E13,120KeV,30° P,4.0E13,80KeV,30° P,2.4E13,80KeV,45°
S/D IIP	As,5.0E15,30KeV	BF2,2.0E15,30KeV

Since the halo region near the drain suppresses the expansion of the depletion layer, it is expected that short channel properties will be improved.

3. Results and Discussion

Vth roll-off characteristics of the halo and the conventional MOSFET are presented in Fig. 2. In the conventional MOSFET, the Vth roll-off characteristics are degraded since the bulk charge depleted by gate voltage is significantly reduced owing to the charge sharing. In case of the halo MOSFET, in contrast, the Vth roll-off characteristics are improved. ΔVth, defined by Vth(Lgate=1.0μm)-Vth(Lgate=0.25μm), with the halo condition becomes small in case of the halo MOSFET as shown in Fig. 3. Fig. 4 shows the breakdown voltage between source and drain(Bvdss) as a function of gate length. In the conventional MOSFET, the surface punchthrough strongly dependent on the Vg is dominated because the drain potential decreases the source-to-substrate potential barrier in the shorter gate length. In case of the halo, however, the Bvdss margin is remarkably improved more than 0.05μm for NMOS and

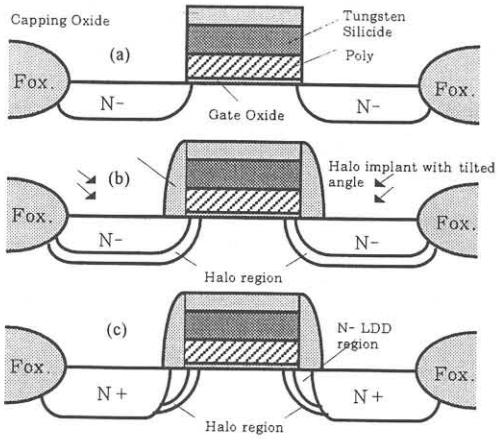

Fig. 1. Process sequence of the halo NMOSFET. (a)N-LDD implant. (b)Halo implant after oxide side-wall formation. (C)N+ source/drain implant.

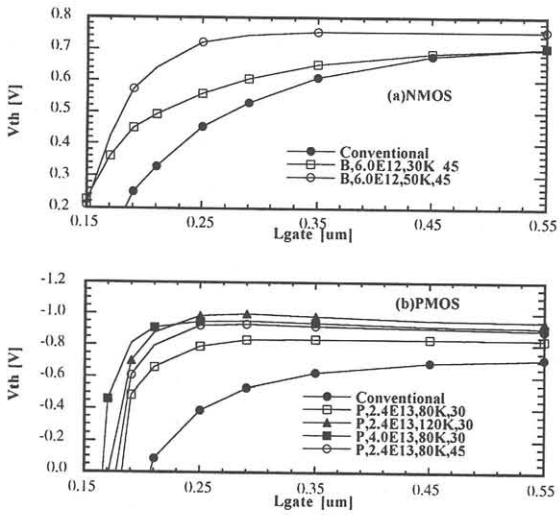

Fig.2. Vth roll-off characteristics as a function of gate length. (a)NMOS. (b)PMOS.

0.12μm for PMOS as compared with that of the conventional MOSFET. Fig. 5 shows the Bvdss characteristics as a function of drain voltage with the |Vg|=0.2V, 0.0V, and -0.2V. The surface punchthrough, as shown in Fig. 5, is remarkably suppressed down to 0.25μm gate length in the halo stucture. These outstanding improvements of punchthrough resistance are considered to be due to the formation of the halo region. Fig. 6 shows the dependence of drain current on gate length. The drain saturation current is measured with |Vds|=2.0V and |Vgs|=2.0V+Vth. The drain saturation current for the halo structure is comparable to that of the conventional MOSFET. As shown in Fig. 6(b), the drain saturation current in the halo PMOSFET is smaller than that of the conventional PMOSFET, for the reason that the combined effect of the blanket N-LDD implantation and the halo implantation increase the source/drain series resistance. Fig. 7 shows the subthreshold swings as a function of gate length for the halo and the conventional MOSFET. The subthreshold swing seriously degrades as gate length decreases in the conventional MOSFET. In case of the halo, however, the subthreshold swing is not deteriorated even though gate length becomes shorter. The subthreshold I-V characteristics for the halo and the conventional devices with Lgate of 0.17μm for NMOS and 0.25μm for PMOS are compared in Fig. 8. The conventional devices severely suffer from drain-induced barrier lowing(DIBL) as the electric field at the drain region can be easily extended to the source region through the depletion region. In contrast, the halo shows much better subthreshold I-V characteristics.

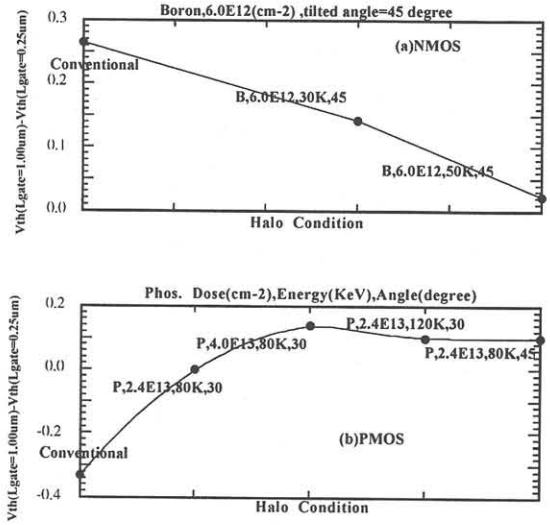

Fig. 3. ΔVth=Vth(Lgate=1.00μm)-Vth(Lgate=0.25μm)with the halo condition. (a)NMOS. (b)PMOS

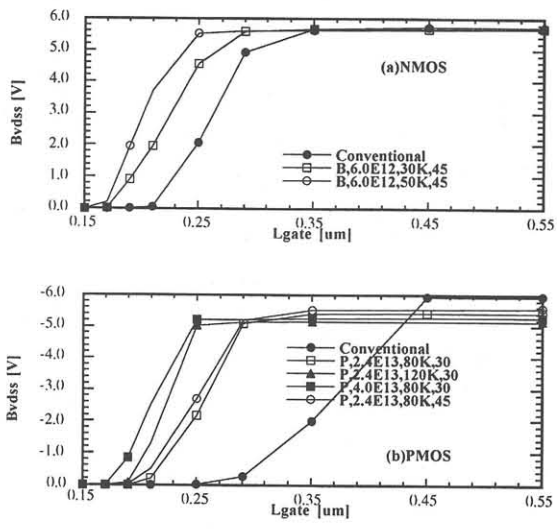

Fig. 4. Breakdown voltage between source and drain as a function of drawn length with 1nA. (a)NMOS. (b)PMOS

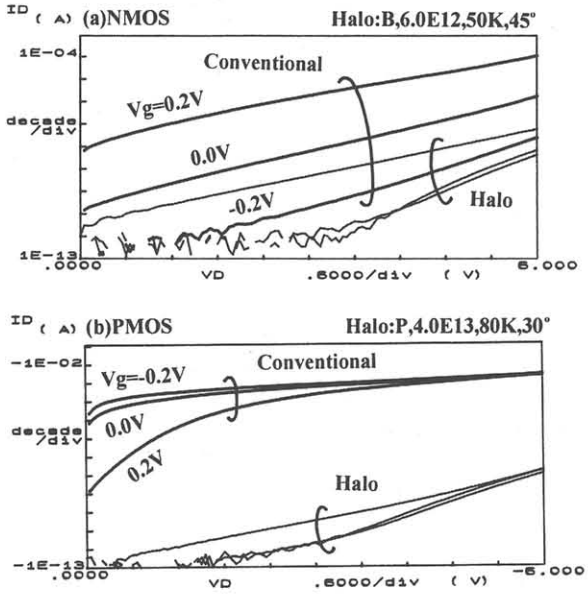

Fig. 5. The Bvdss characteristics as a function of drain voltage with |Vg|=0.2V,0.0V ,and -0.2V. (a)NMOS. with Lgate=0.25μm. (b)PMOS with Lgate=0.25μm.

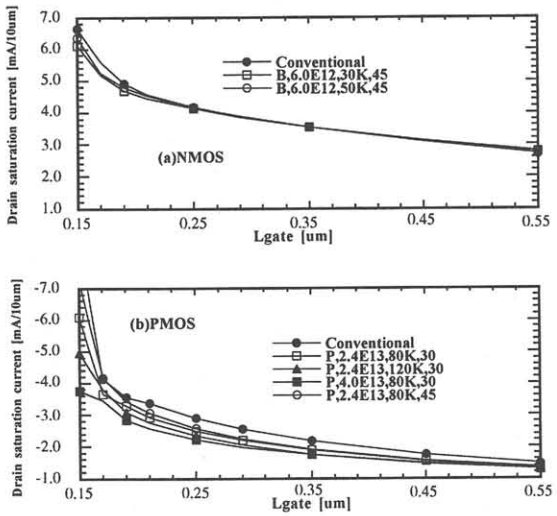

Fig. 6. Drain saturation current as a function of gate length. Drain voltage is 2.0V and gate voltage is 2.0V+Vth. (a)NMOS. (b)PMOS.

4. Conclusion

A novel halo technology has been developed. The major feature of this process for halo CMOSFET is that halo implantation is performed without additional implantation masks. The Vth roll-off characteristics of the halo MOSFET are drastically suppressed as compared with those of the conventional MOSFET. The Bvdss margin is remarkably improved more than 0.05μm for NMOS and 0.12μm for PMOS as compared with that of conventional MOSFET. The drain saturation current of halo is comparable to that of conventional NMOSFET. The halo shows excellent subthreshold I-V characteristics. Hence, a 0.25μm CMOSFET becomes practical for highly manufacturable 1 Gb DRAM.

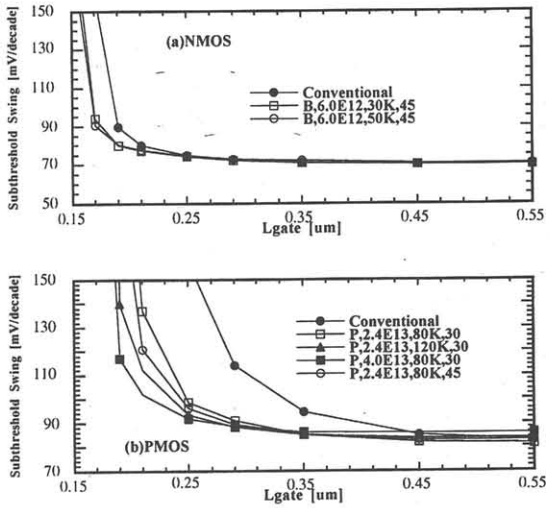

Fig. 7. The subthreshold swing as a function of gate length. (a)NMOS. (b)PMOS.

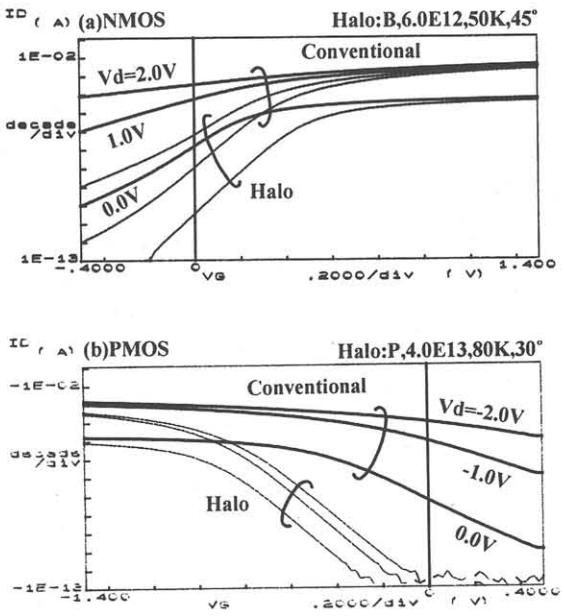

Fig. 8. Subthreshold I-V characteristics with |Vd|=0.0V, 1.0V, and 2.0V. (a)NMOS with Lgate=0.17μm. (b)PMOS with Lgate=0.25μm.

5. References

1). E. Takeda, G. A. C. Jones, and H. Ahmed, IEEE Electron devices, **32**(1985)322.

2). S. Ogura, C. F. Codella, N. Rovedo, J. F. Shepard, and J. Riseman, IEDM *Tech. Dig.*, (1982)718.

3). C. F. Codella, and S. Ogura, IEDM *Tech. Dig.*, (1985)230.

4). Y. Okumura, M. Shirahata, T. Okudaira, A. Hachisuka, H. Arima, T. Matsukawa, and N. Tsubouchi, IEDM *Tech. Dig.*, (1990)391.

5). A. Hori, A. Hiroki, H. Nakaoka, M. Segawa, and T. Hori, IEEE Trans. Electron Devices, **42**(1995)78.