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Substrate Engineering for Reduction of α-Particle-Induced Charge Collection Efficiency

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Measurements of α-particle-induced charge collection efficiency (CCE) together with simulation analysis have been made for the several types of substrates, expected to have low CCE. CCE for the double well is low because the bottom n-layer acts as an effective electron absorber. For the epi-substrate, CCE increases with increase in the thickness of the epi-layer because of the potential difference between the heavily doped substrate and the epi-layer. CCE for the p-well with the MeV implanted buried layer is low because of short carrier life time in the layer.

1. INTRODUCTION

One of the severest problems for DRAM is decrease in soft error immunity due to the scaling of the stored charge in low voltage operation or in further increase of the integration density, since the collection efficiency of minority carriers induced by an incident α-particle essentially scales with neither the size of a device nor the supply voltage. Reduction of soft error rate should be achieved by the substrate engineering that can reduce α-particle-induced charge collection efficiency (CCE). Schemes for suppressing CCE may be summarized as follows; (1) preventing minority carriers from traveling toward the diffusion layer; (2) absorbing minority carriers by an extra-fabricated layer; (3) killing minority carriers before they reach the diffusion layer. In this paper we will present the results of the measurements of CCE as well as the analysis by simulation for several substrate structures which are shown in Fig. 1. Fig. 1 (a) shows MeV implanted retrograde well which is considered to be one of the technique realizing the scheme (1) since a potential barrier inside the substrate prevents electrons from moving toward the diffusion layer[1]. We intended to have lower CCE for the other substrates than for this simple retrograde p-well. Fig. 1 (b) shows double well which is based on the scheme (2). Fig. 1 (c) and (d) shows, respectively, p-well on epi-substrate and p-well with MeV implanted heavily doped buried layer[2,3] which are based on the scheme (3).

2. EXPERIMENTAL PROCEDURE

Fig. 2 shows a schematic diagram of the experimental setup. An 1 mm × 5 mm flat n^+ / p junction at the reverse bias

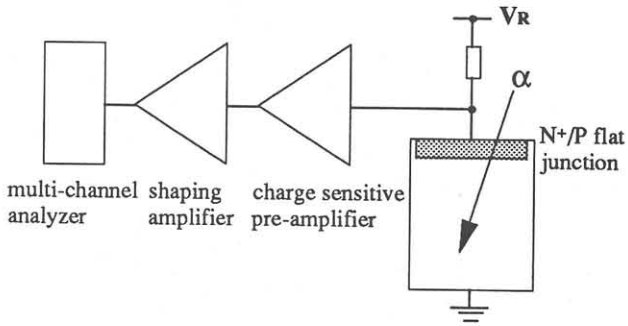

Fig. 2. Schematic diagram of the apparutus for the measurements of α-particle-induced-charge collection efficiency (CCE).

5 V is irradiated by α-rays from an ^{241}Am source. The output signal is fed into a multi-channel analyzer after amplified and differentiated by a charge-sensitive pre-amplifier and a shaping amplifier. CCE is determined by the peak value of the pulse height spectrum. We normalized the measured CCE by the CCE for the simple retrograde p-well to cancel out the systematic fluctuation of the measurement.

3. RESULTS AND DISCUSSION

3. 1 Double well

Fig. 3 shows the measured CCE for the double well which has a depth of 2 μm or 3 μm. CCE for the double well is much lower than that for the simple retrograde p-well. The action of the bottom n-layer as an electron absorber was confirmed by simulation. In the simulation, α-particle is injected perpendicular to the substrate and the time

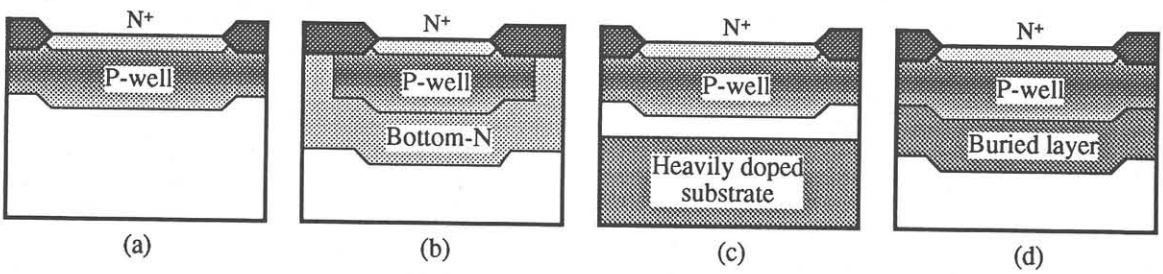

Fig. 1. Substrate structures under investgation; (a) simple retrograde p-well, (b) double well, (c) simple retrograde p-well on epitaxial wafer, (d) retrograde p-well with MeV implanted buried layer.

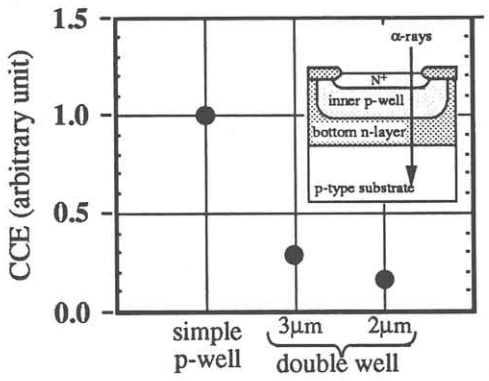

Fig. 3. α-particle-induced-charge collection efficiency (CCE) for the double well of 2 μm or 3 μm depth; normalized by CCE for the simple p-well.

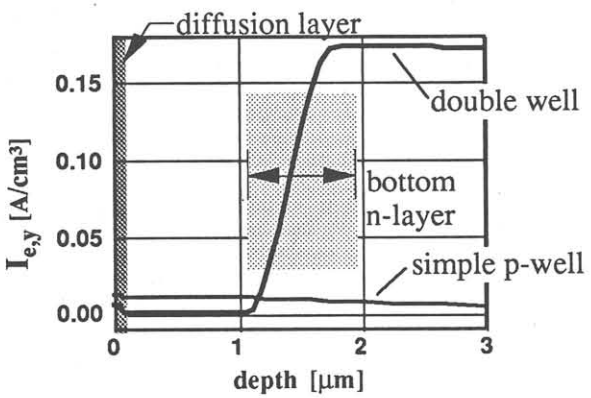

Fig. 4. Simulated electron current density toward the n+ diffusion layer ($I_{e,y}$) after 10 ns for the double well and the simple p-well.

development of two-dimensional internal state was calculated. Differences of the mechanism of charge collection among the substrate structures are analyzed mainly by comparing the electric current density toward the diffusion layer (*Ie,y*) and the electron density (*Ne*) along the track of α-particle. Fig. 4 shows *Ie,y* after 100 ns from the injection of α-particle. *Ie,y* near the diffusion layer is much less for the double well than for the simple p-well. The bottom n-layer is found to act as an effective electron absorber. From the experimental result that CCE for the double well of 2 μm depth is lower than that for the double well of 3 μm depth, it is considered to be more effective to put an absorptive bottom n-layer near the surface.

3. 2 P-well on epi-substrate

CCE for the epi-substrate may be expected to be lower than that for the non-epi-substrate since the carrier life time in a heavily doped substrate is shorter than that in a lightly doped substrate. In the case for minority carriers induced by an α-particle, the recombination rate is dominated by Shockley-Read-Hall term which is expressed as follows;

$$R^{SRH} = \frac{np - n_i^2}{\tau_p(n + n_i) + \tau_n(p + n_i)}$$

$$\tau_p = \frac{\tau_{p0}}{1 + C_i / N_{ref}^i}, \quad \tau_n = \frac{\tau_{n0}}{1 + C_i / N_{ref}^i}$$

where n is the electron density, p is the hole density, n_i is the intrinsic carrier density, C_i is the impurity density and τ_{p0}, τ_{n0} and N_i^{ref} are the constants. Considering $p > n >> n_i$, R^{SRH} is reduced to

$$R^{SRH} \sim \frac{n}{\tau_n}.$$

Thus we can estimate the life time of excess electrons in the substrate is given by $\cong \tau_n$. By substituting reasonable values[4,5], we get $\tau_{n,non\text{-}epi} \cong 3.1 \times 10^{-5}\ s$ for the lightly doped substrate and $\tau_{n,epi} \cong 1.4 \times 10^{-7}\ s$ for the heavily doped substrate. If the charge collection takes much longer than $\tau_{n,non\text{-}epi}$, CCE for the epi-substrate should become lower than that for the non-epi-substrate. Fig. 5 shows the measured CCE for p-well on epi-substrates. The thickness of epi-layers ranges from 2 μm to 8 μm. CCE for the 2 μm epi-substrate is lower than that for the non-epi-substrate. CCE for the epi-substrates of more than 3 μm epi-layer is, however, higher than that for non-epi-substrate and CCE increases with the thickness of epi-layer. Fig. 6 shows a simple model to explain the relation between CCE and the thickness of an epi-layer. In the epi-substrate, the potential difference exists between the heavily doped substrate and the lightly doped epi-layer. This potential difference acts as a barrier that prevents electrons from traveling into the substrate. Fig. 7 shows simulated *Ne* after 100 ns for the 5 μm epi-substrate. *Ne* in the epi-layer is rather higher than *Ne* in the non-epi-substrate. These electrons are to be eventually collected to the diffusion layer. The simulation also shows that charge collection completes within at most $10^{-6}\ s$, that is consider to be too short to make the effect of the heavily doped substrate clear.

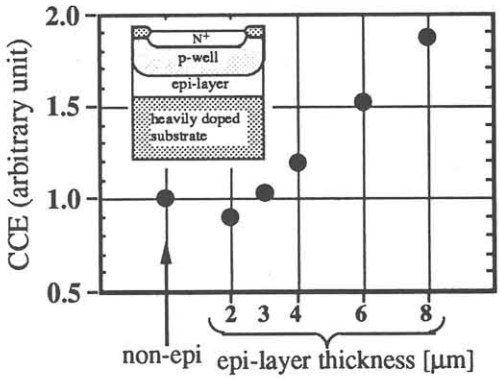

Fig. 5. CCE for the simple p-well on epi-substrate; normalized by CCE for the simple p-well on non-epi-substrate.

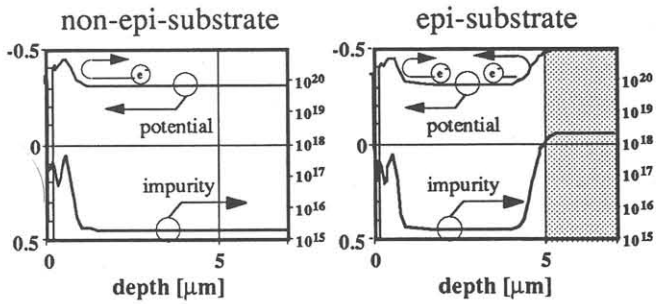

Fig. 6. Impurity profiles and potentials for the epi-substrate and the non-epi-substrate. For the epi-substrate, the potential difference acts as a barrier for electrons.

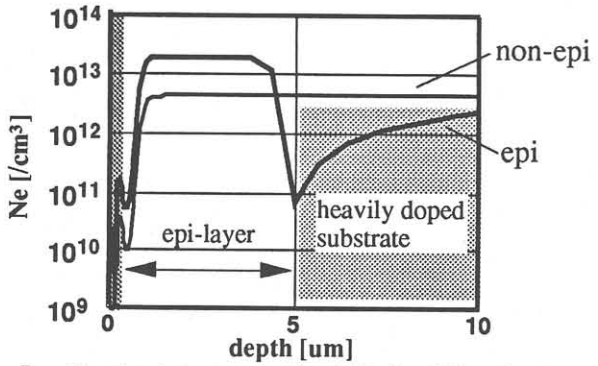

Fig. 7. Simulated electron density (*Ne*) after 100 ns for the epi-substrate and the non-epi-substrate

3. 3 P-well with MeV implanted buried layer

Fig. 8 shows the measured CCE for p-well with a heavily doped buried layer. The buried layers were formed by high dosage MeV implantation of Si^+ or B^+. CCE for the p-well with the buried layer is much lower than that for the simple p-well. Lattice defects introduced by the high dosage MeV implantation are considered to play an important role since silicon implantation as well as boron implantation reduces CCE. Fig. 9 is a TEM micrograph that shows lattice defects by high dosage Si^+ implantation. We simulated the role of the buried layer by introducing the additional SRH-type GR-term locally in the substrate. Fig. 10 shows the simulated *Ie,y* after 10 ns from the incidence of α-particle for p-well with a buried layer. In the buried layer, carrier life time was set to be short by introducing the additional GR-term in which $\tau_{n0,p0}' = r \times \tau_{n0,p0}$ are substituted in place of $\tau_{n0,p0}$ in the R^{SRH} expression, where r is the shortening factor of the carrier life time. *Ie,y* near the diffusion layer appreciably decreases when r is set less than 10^{-4} and becomes comparable to *Ie,y* for the double well if the carrier life time in the buried layer is ~ 10^{-11} s. The buried layer was confirmed to act as an effective minority carrier killer, though we have little data to relate quantitatively the results of the simulation with the carrier life time in the defects region as shown in Fig. 9.

4. CONCLUSION

Measurements of α-particle-induced charge collection efficiency (CCE) together with simulation analysis have been made for the double well, the p-well on the epi-substrate and the p-well with the heavily doped buried layer.

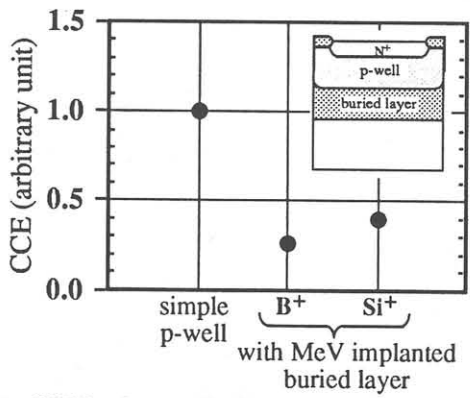

Fig. 8. CCE for the p-well with the heavily doped buried layer; normalized by CCE for the simple p-well.

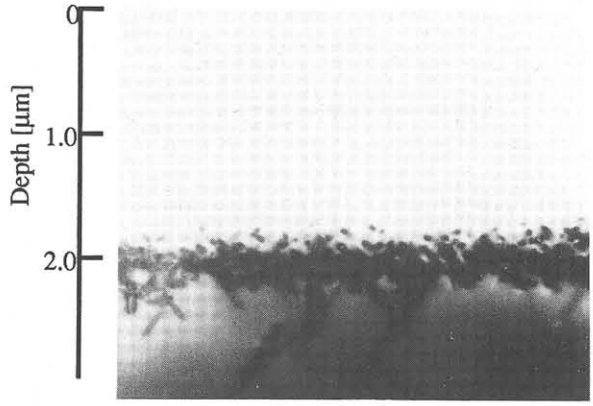

Fig. 9. Cross-sectional TEM micrograph. Si^+ implantation 2.4MeV 1E15 /cm²

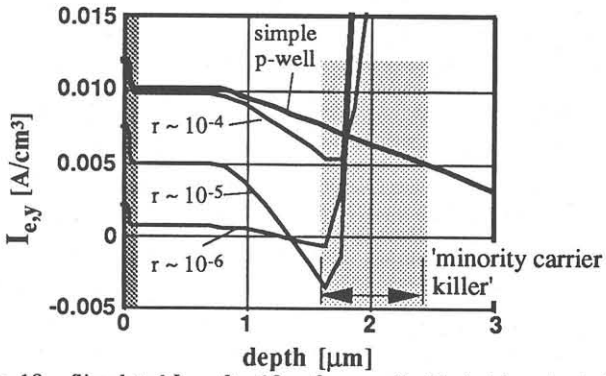

Fig. 10. Simulated *Ie,y* after 10 ns for p-well with / without buried 'minority carrier killer'. *r* is life time shortening factor in the additional SRH-type GR-term (see text).

CCE for the double well is low because the bottom n-layer acts as an effective absorber for minority carriers. CCE for the p-well on the epi-substrate increases with increase in the thickness of the epi-layer because potential difference between the heavily doped substrate and the lightly doped epi-layer forms a barrier which prevents electrons from traveling into the substrate. Even for the p-well on the thin epi-layer CCE is comparable to that for the p-well on the non-epi-substrate, since charge correction doesn't take longer time than the carrier life time in the heavily doped substrate. CCE for the p-well with the MeV implanted heavily doped buried layer is as low as that for double well because the carrier life time is short in the buried layer due to lattice defects. It is more effective to put the bottom n-layer or the buried layer near the surface to reduce CCE.

Acknowledgment

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