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A Comparative Study of Interface Trap Induced Drain Leakage Current in Various n-MOSFET Structures

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Various drain leakage current mechanisms via hot carrier stress generated interface traps are modeled and characterized in a 0.5μm LATID n-MOSFET and a 2.0μm S/D n-MOSFET. Both of electron and hole tunneling and thermionic emission are considered. In a band-trap-band tunneling dominant condition, a $\mathbf{B_{it}}$ about 13MV/cm was obtained in the LATID MOSFET while a $\mathbf{B_{it}}$ of 25MV/cm was extracted in the S/D MOSFET structure. The variation of the $\mathbf{B_{it}}$ suggests a different tunneling barrier height in the two strcutures.

I. Introduction

Vertical tunneling in thin gate oxide MOSFET's (GIDL) has been long recognized to be a major drain leakage mechanism in off-state MOSFET's [1]. As the device dimension is continually scaled down, the lateral field enhanced tunneling may also play an important role in the drain leakage current in some MOSFET structures. Recently, it has been shown that the drain leakage is seriously worsened due to hot carrier stress generated interface traps [2,3]. In our earlier work, an interface trap-assisted tunneling and thermionic emission model [4] has been developed to evaluate an increased drain leakage current after hot carrier stress. In the model, a complete band-trap-band leakage path is formed at the Si/SiO2 interface by hole emission from interface traps to a valence band and electron emission from interface traps to a conduction band. Both hole and electron transitions are carried out through quantum tunneling or thermal excitation. Fig. 1 shows the various carrier transition processes schematically. At a low drain-to-gate bias (V_{dg}), our model reduces to the well-known Shockley-Read-Hall (SRH) theory and thermal generation of electron-hole pairs is dominant. As V_{dg} increases, a thermionic-field emission mechanism, or the so-called band-to-defect model proposed by Hori [5], becomes a major leakage path. At a sufficiently large V_{dg}, band-trap-band tunneling holds responsible for a drain leakage.

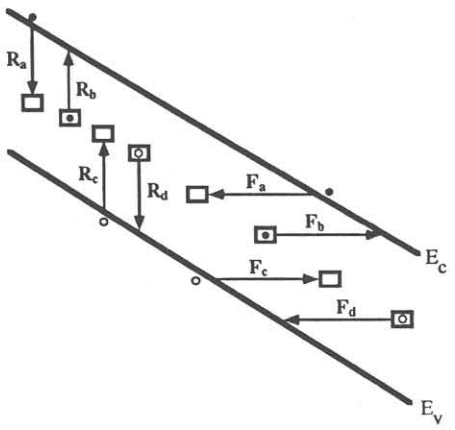

Fig. 1 Various electron and hole transition mechanisms through interface traps.

II. Device Structures

Two types of device structures, a 0.5μm LATID n-MOSFET and a 2.0μm conventional S/D n-MOSFET were fabricated to manifest the drain leakage characteristics in two limits; The gate oxide thickness of the 0.5μm LATID is 150Å and thus the lateral field is stronger in the interface trap generation region. On the other side, the thickness in the 2.0μm S/D structure is chosen to be 90Å to demonstrate the vertical field induced tunneling characteristics. To obtain a maximum interface trap generation rate [6], we adopt a maximum substrate current stress method.

III. Results and Discussions

In order to evaluate various transition process shown in Fig. 1, possible combinations of a drain leakage path are listed in Table 1 which include hole tunneling followed by electron tunneling ($\mathbf{I_{tt}}$), hole tunneling followed by electron thermionic emission ($\mathbf{I_{tg}}$), hole thermionic emission followed by electron tunneling ($\mathbf{I_{gt}}$), and hole thermionic emission followed by electron thermionic emission ($\mathbf{I_{gg}}$). These four components of the drain leakage current in the off-state S/D MOSFET are characterized and modeled in Fig. 2. Also indicated in the figure are the dominant regions of the two-step tunneling, the thermionic field emission and the SRH thermal generation, respectively. The feature of the measured current (solid curve) matches the calculated characteristics well. Furthermore, in the two-step tunneling dominant condition in Fig. 2, it can be shown that the increased drain leakage current due to interface traps can be adequately described by [4]

$$\Delta I_d = A\exp(-B_{it}(E_t)/F) \qquad (1)$$

$$B_{it}(E_t) = \frac{4}{h}(2m_n)^{1/2}\ \frac{(E_c-E_t)^{3/2}}{3q} \qquad (2)$$

Table 1 Various interface trap-assisted leakage components.

Hole transition	Electron transition	Leakage current component
Tunnel	Tunnel	ΔI_{tt}
Tunnel	Thermal	ΔI_{tg}
Thermal	Tunnel	ΔI_{gt}
Thermal	Thermal	ΔI_{gg}

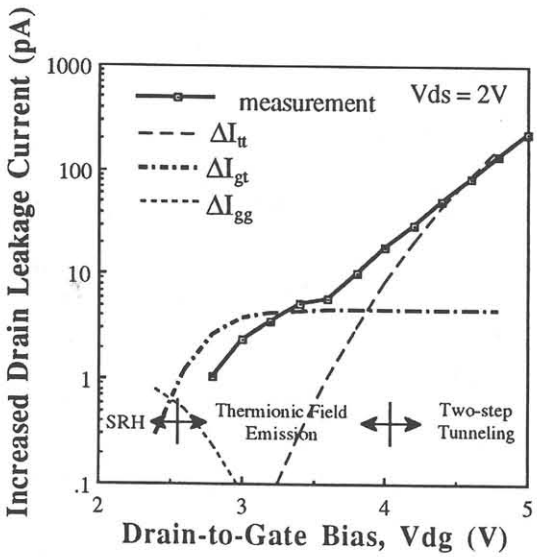

Fig. 2 Comparison of various leakage components in the S/D MOSFET.

$$E_t = \frac{E_v + (F_l/F)^{2/3} E_c}{1 + (F_l/F)^{2/3}} \qquad (3)$$

where A is proportional to the interface trap density, F_l is a lateral field, F is a total field, and $\mathbf{E_t}$ is the energy level of interface states which are most effective in the band-trap-band tunneling process. It should be pointed out that if the lateral field is much greater than the vertical field, the theoretically lower limit of $\mathbf{B_{it}}$ is about 13 MV/cm and the corresponding $\mathbf{E_t}$ is $0.5(\mathbf{E_c}+\mathbf{E_v})$. In the other extreme, if the vertical field is much larger than the lateral field, $\mathbf{B_{it}}$ has a maximum value of 36MV/cm which is the same as the GIDL [4]. Fig. 3 shows the drain leakage currents before and after hot carrier stress in the two structures. The additional drain leakage current through the band-trap-band leakage path is shown in Fig. 4. The reader should be reminded that the two-step tunneling is a dominant leakage mechanism in the bias condition in Fig. 4. The measured and calculated **Bit** versus gate bias are shown in Fig. 5. In the LATID structure, the lateral field is dominant and thus its **Bit** is close to the theoretically lower limit. In the S/D structure, the vertical field is larger in the interface trap region. Therefore, the vertical field induced tunneling is dominant and the **Bit** reaches a higher value, as shown in Eq. (2). In reality, the **Bit** reflects a potential barrier height in tunneling and the measured **Bit** obtained in the LATID MOSFET is an evidence of midgap trap assisted tunneling. Moreover, we shift the interface distribution **Nit** along the channel in the LATID structure to investigate the sensitivity of the $\mathbf{B_{it}}$ to the interface trap position. The result is shown in Fig. 6. There exists a window in which the $\mathbf{B_{it}}$ is almost unchanged. This suggests that once the generated interface traps are located in the window, a theoretically lower limit of the **Bit** should be obtained.

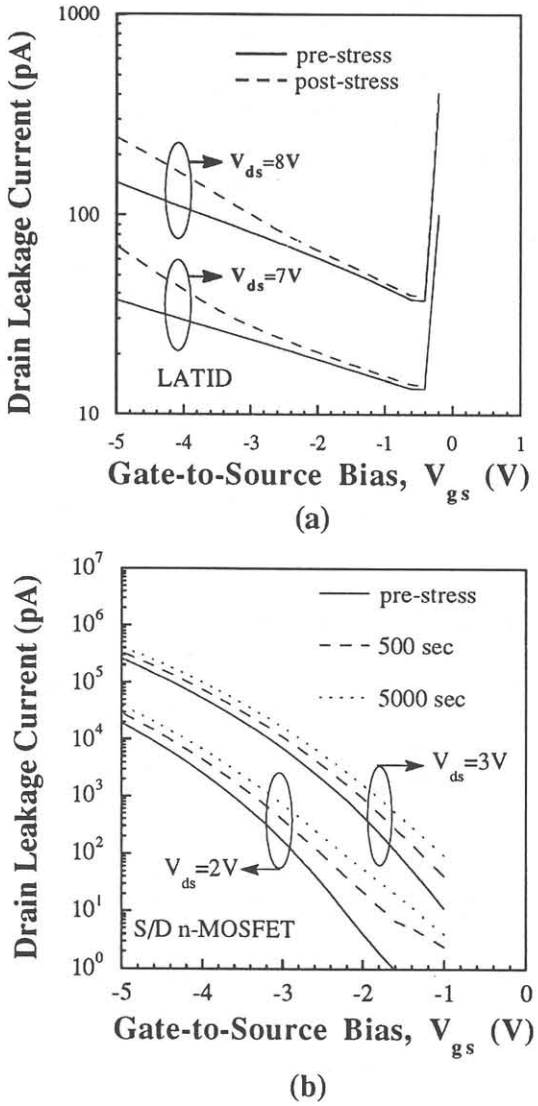

Fig. 3 Measured drain leakage currents before and after hot carrier stress (a) LATID (b) S/D.

Acknowledgement

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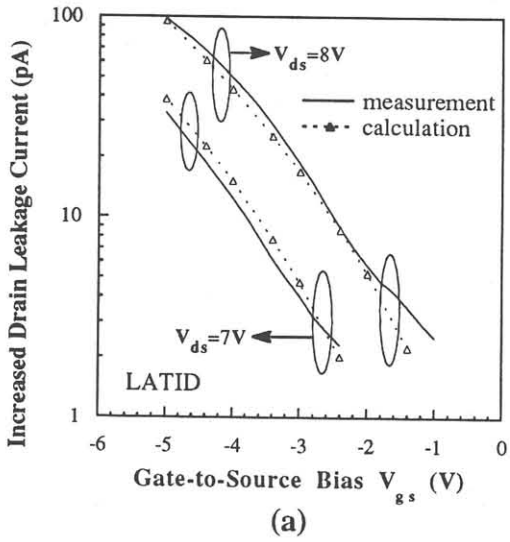


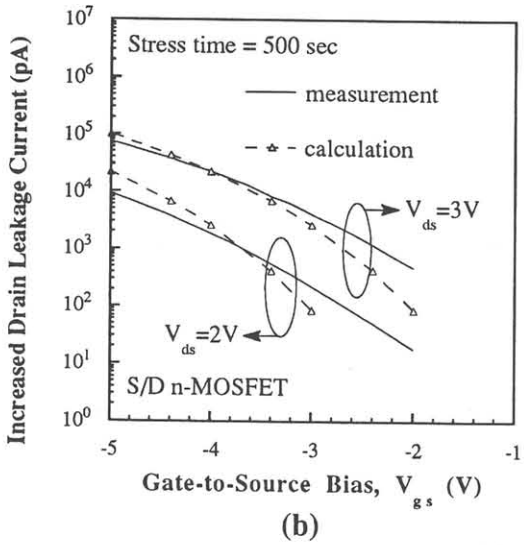
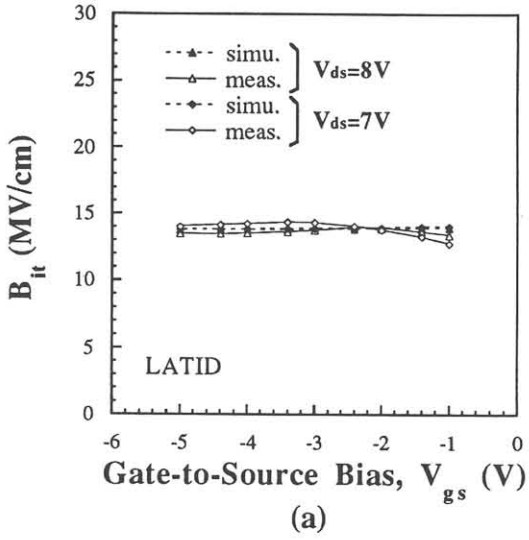


Fig. 4 Measured and calculated additional drain leakage due to interface traps (a) LATID (b) S/D.



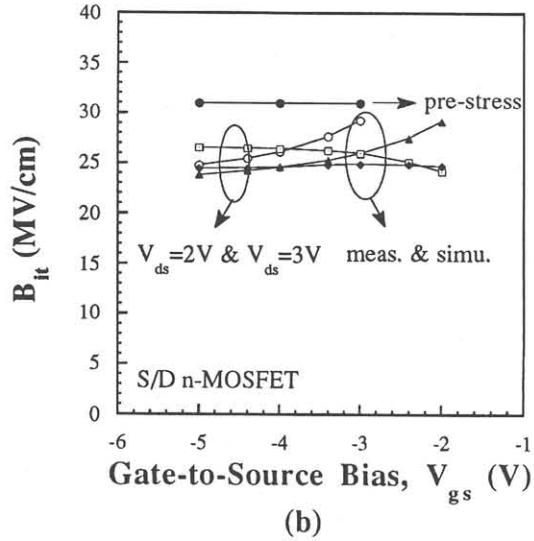


Fig. 5 Measured and calculated Bit versus gate bias (a) LATID (b) S/D.

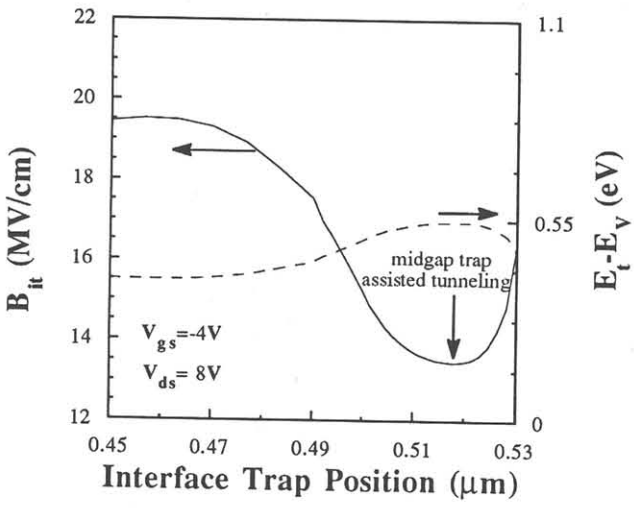


Fig. 6 The dependence of Bit and effective trap energy on the trap position in the LATID MOSFET.