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Reliability of Non-Uniformly Doped Channel (NUDC) MOSFETs for Sub-Quarter-Micron Region

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This paper presents the analysis of hot carrier degradation of NUDC MOSFETs. Simulation has been performed in order to investigate the influence of the NUDC structure on device characteristics. It is demonstrated that the hot carrier resistance of the NUDC MOSFETs is quite comparable to that of the conventional MOSFETs for low voltage operation using thin gate oxide. This reason is explained by the drain electric filed strength of the NUDC MOSFETs, which is the same as that of the conventional MOSFETs due to the thin oxide, since the drain electric field is not only affected by the channel impurity but also strongly influenced by the gate electrode.

1. INTRODUCTION

There has been increasing attention on the low voltage operation of CMOS and much effort has been made on the development of MOSFET structures which can realize low threshold voltages. For this purpose several non-uniform channel structures have been so far proposed such as the NUDC MOSFETs[1] and similar structures utilizing pocket implant[2]. However there has been almost no report in detail for hot carrier degradation in spite of the big concern for this structure. Hence we will present the analysis of hot carrier degradation of the NUDC MOSFETs here. We will also present the most suitable non-uniform channel structure for low voltage operation.

2. SIMULATION ANALYSIS

Simulation has been performed in order to investigate the influence of the NUDC structure on device characteristics. Ideal impurity profile was used for simulation as shown in Fig.1. The region I is a p-type channel region of low

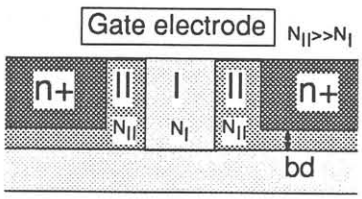

Fig.1 Schematic cross-section for simulation.

concentration and the region II is what is called an NUDC layer having high p-type impurity concentration to suppress punch-through. N_I and N_{II} are the impurity densities of the region I and II, respectively. bd is the excess of an NUDC layer over the source/drain depth. Fig.2 shows the Vth as a function of the ratio $L_I/(L_I + L_{II})$ obtained by simulation where L_I and L_{II} are lengths of the region I and II. N_{II} required to prevent punch-through is also presented in Fig.2. It is noted that Vth can be reduced by increasing the ratio of L_I, and simultaneously by increasing N_{II}. This small Vth voltage can be obtained because the average channel concentration over the whole channel can be reduced by increasing the ratio of L_I in spite of the increase in N_{II}. However this high concentration N_{II} may increase the drain electric field, thereby reducing hot carrier resistance. We accordingly analyzed the internal electric field. Firstly we investigated the depth dependence of the NUDC layer on the junction electric field. Fig.3 shows the bd dependence on the maximum junction electric field Emax at the drain region and Fig.4 shows the bd dependence on the extension of the equi-potential line from the drain. The Emax increases

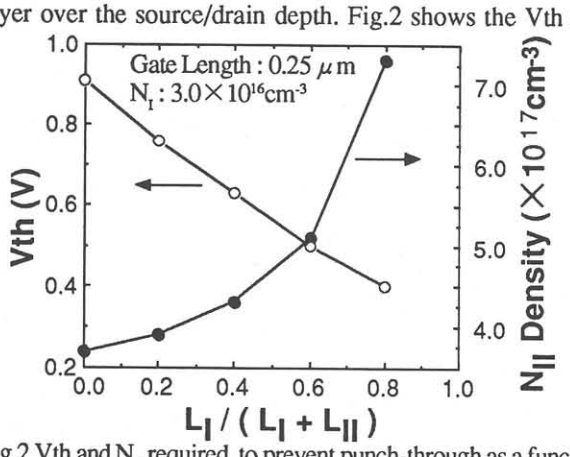

Fig.2 Vth and N_{II} required to prevent punch-through as a function of the ratio $L_I/(L_I + L_{II})$.

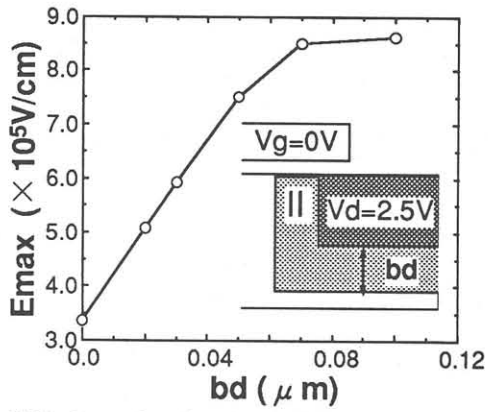

Fig.3 Maximum junction electric field as a function of bd.

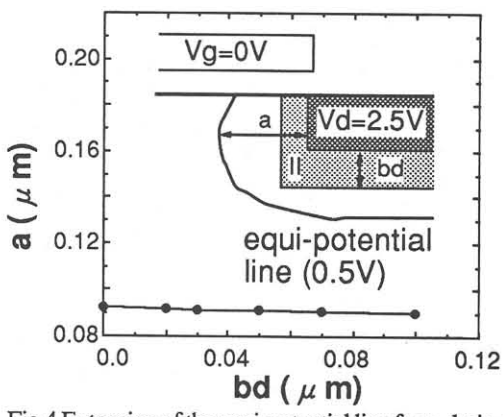

Fig.4 Extension of the equi-potential line from drain as a function of bd.

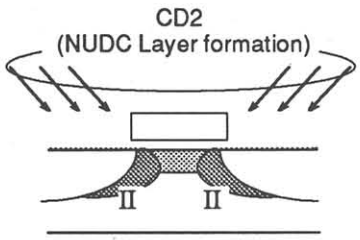

Fig.5 Cross Sectional View of the NUDC MOSFET fabricated by the oblique rotational implantation.

with bd, while the punch-through does not depend on bd. Therefore the depth of the NUDC layer can be within the drain junction depth to suppress the punch-through, which can avoid the increase in the junction electric field. Secondly we investigated the drain electric field having the impurity profiles obtained by simulation. As shown in Fig.5, after the gate electrode definition, NUDC layer formation is performed by the oblique rotational boron implantation, what we call CD2. The calculated simulation profiles are shown in Fig.6. NUDC MOSFET certainly has a non-uniformly doped channel profile while the conventional MOSFET has a uniform impurity profile along the channel.

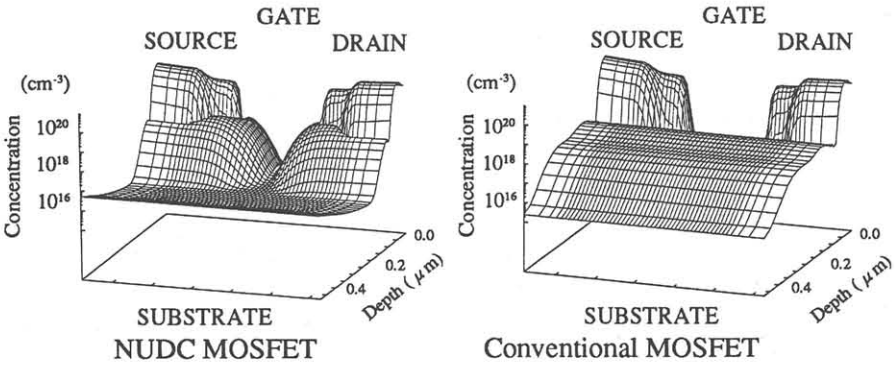

Fig.6 Calculated impurity profiles of the NUDC and conventional MOSFETs.

The comparison between the two channel profiles at the surface is shown in Fig.7 where the gate electrode lies from x=0.0 μm to 1.2 μm over the gate oxide. The NUDC MOSFET has approximately an order higher impurity

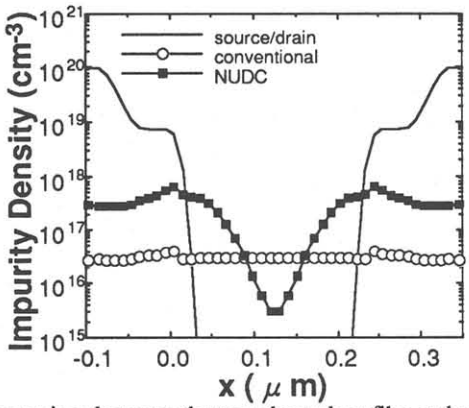

Fig.7 Comparison between the two channel profiles at the surface.

density near the drain region. In Fig.8 we show the drain electric field distributions of the NUDC MOSFET and the conventional MOSFET. It should be noted that the maximum electric fields of both MOSFETs are almost identical though the channel impurity profiles are quite different. To explain this, we estimated the drain electric field due to the gate electrode analytically using the

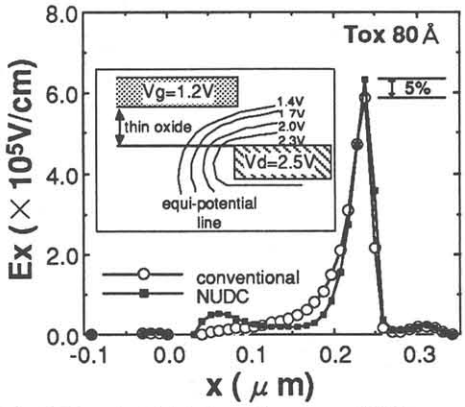

Fig.8 Electric Field along the channel (thin gate oxide).

cylindrical coordinate as shown in Fig.9 on the assumption that the potentials are constant on x-coordinate and y-coordinate. Since we also assumed that there is no space charge, the potential distribution approximately does not depend on r. The Laplace equation is consequently given as

$$\frac{\partial^2 V}{\partial \psi^2} = 0 \qquad (1)$$

It can be solved under the boundary conditions

$$\begin{cases} V(\psi = 0) = Vd \\ V(\psi = \pi/2) = Vg \end{cases} \qquad (2)$$

We also estimated the junction electric fields for two abrupt junctions. As a result of the estimation shown in Fig.9, the drain electric field due to the gate electrode is comparable to the junction fields when the gate oxide is thin. It can be said that the drain electric field is not only affected by the channel impurity but also strongly influenced by the gate electrode. Fig.10 shows the result calculated under the same condition as in Fig.8 except that the gate oxide is thick (1 μm) to eliminate the influence of the gate electrode. Reflecting the difference in the channel impurity concentration, the maximum electric field of the NUDC MOSFET is approximately 1.5 times as high as that of the conventional MOSFET. As presented in Fig.8, with decrease in the gate oxide thickness, the maximum field for both of the two

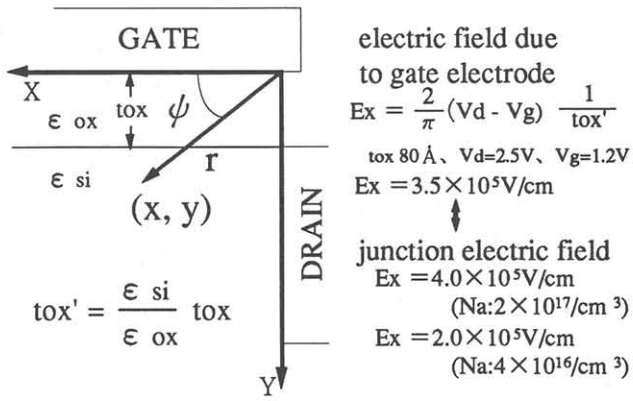

Fig.9 Comparison between electric field due to gate electrode and junction electric field.

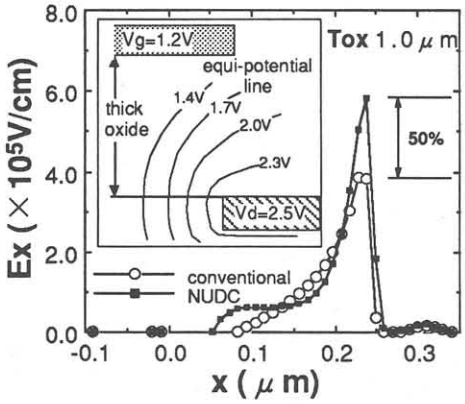

Fig.10 Electric Field along the channel (thick gate oxide).

MOSFETs increases, resulting in the little difference in the electric field between the two MOSFETs. Hence the hot carrier resistance of the NUDC MOSFET becomes comparable to that of the conventional MOSFET for low voltage operation using thin gate oxide.

3. EXPERIMENTAL RESULTS

We fabricated NUDC MOSFETs based on the simulation analysis. The implant for CD2 consists of the implant energy of vertical component about 20keV, the tilt angle of 20~40°, and the dose of $0.5\sim1.3\times10^{13}/cm^2$ with boron ion. The gate oxide thickness is 80Å. For the comparative study, the conventional MOSFETs were fabricated with channel implant before the gate electrode formation. Fig.11 depicts

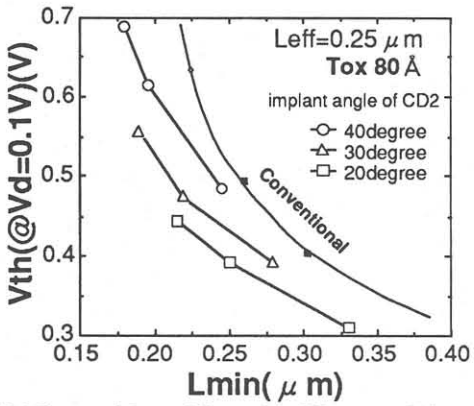

Fig.11 Measured data of the trade-off between Vth and Lmin.

the measured data for the trade-off between Vth and Lmin. Lmin is defined as a minimum channel length beyond which the drain punch-through voltage can exceed the supply voltage. For the same Lmin, the smaller the implant angle of CD2, the lower the Vth can be as expected from the simulation results. Fig.12 shows short channel characteristics of the NUDC MOSFETs with CD2 20keV 20° $1.25\times10^{13}/cm^2$. Vth and drain current as a function of gate length are shown in Fig.12. It is apparent that the NUDC MOSFET can realize low Vth and high current drivability as compared with the conventional MOSFET. Fig.13 shows hot-carrier-induced drain current degradations and Vth shifts as a function of stress time. There is little difference between the NUDC MOSFET and the conventional MOSFET. As explained previously, the reason is the little difference in the drain electric field between the two MOSFETs which have thin gate oxide.

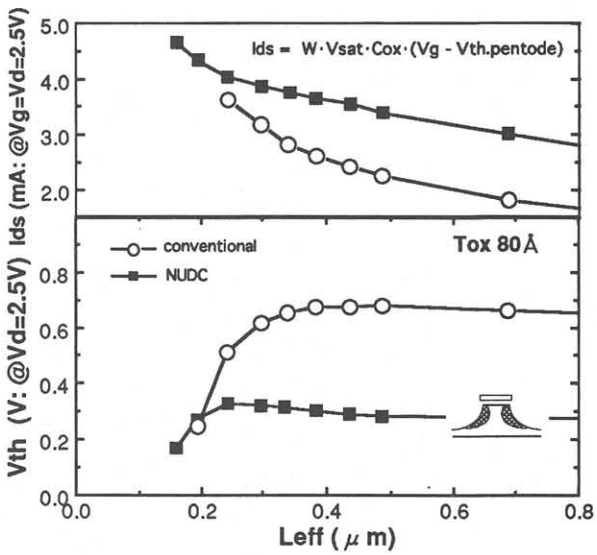

Fig.12 Vth roll-off and drain current of the transistor for CMOS logic operation.

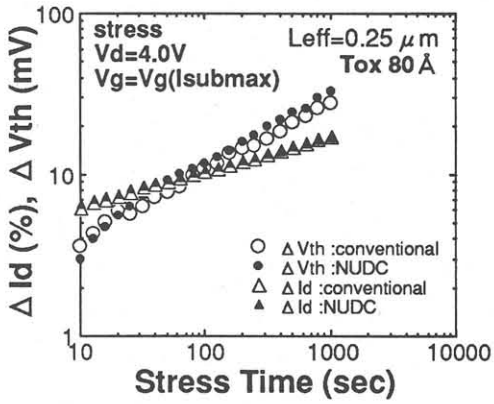

Fig.13 Hot-carrier-induced Id degradation as a function of time.

4. CONCLUSION

We demonstrated that the hot carrier resistance of the NUDC MOSFET is quite comparable to that of the conventional MOSFET. This reason is explained by the fact that the drain electric field of the NUDC MOSFET can be the same as that of conventional MOSFET due to the gate electric field. Furthermore we clarified that the NUDC structure is suitable structure for low voltage operation even in the sub-quarter micron region.

ACKNOWLEDGMENT

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2) A.Chatterjee et al., IEDM Tech. Dig. (1994) 87.