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An Experimental Study of Impact Ionization Phenomena in Sub-0.1μm Si MOSFETs

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The impact ionization phenomena in sub-0.1μm Si N-MOSFET has been examined in detail. Sub-band gap impact ionization can be observed for 0.08μm Nch-MOSFET, and the minimum drain voltage where the substrate current can be observed is lower for thicker gate oxide device. Although thin gate oxide suppresses impact ionization, the gate oxide thickness dependence of the impact ionization is decreased as the gate length becomes short.

Introduction

The scaling trend in CMOS devices has significantly improved LSI performance over the past twenty years. Miniaturization of Si MOSFETs is a most powerful method to improve device performance. The scaling limitation in Si devices is a key issue in the VLSI development. The possibility of sub-0.1μm CMOS, the supply voltage, the limitation of performance are great concerns for VLSI research and development scene.

However small geometry MOSFETs suffer from a reliability problem such as hot carrier effect, which induces the threshold voltage shift and transconductance degradation. Recently, many researchers have reported the hot carrier effect of sub micron MOSFETs and a few studies have been done for 0.1μm-MOS devices. However, none of them have discussed the gate oxide thickness dependence on the impact ionization in detail.

In this paper, we have evaluated the gate electric field effect to impact ionization in sub-0.1μm Si MOSFETs, by analyzing the gate oxide thickness dependence in N MOSFETs with gate length less than 0.1μm.

Device Fabrication

Nch-MOSFETs with the gate oxide of 4nm, 6nm and 8nm were fabricated. Starting material was a p-type silicon CZ-substrate. First well implant and LOCOS isolation were performed followed by channel implantation. The impurity concentration of the well and channel were very low. The gate oxide was formed by pyro oxidation. The thickness is 4, 6 and 8nm. After formation of the polysilicon gate electrode, boron ion (pocket) was implanted using the gate electrode as a mask(1), and hence the impurity concentration of the three kinds of test devices were identical. The implantation condition is BF2, 100KeV, 1 x $10^{13}cm^{-2}$.

The source/drain extension was utilized. The 15KeV Arsenic ions were implanted with a dose of 1 x $10^{14}cm^{-2}$, and the impurity concentration is more than 1 x $10^{19}cm^{-3}$. The deep source/drain were formed with the oxide side wall of 120nm. All the process conditions were identical for three devices except for the gate oxide thickness. Fig.1 shows cross sectional view of the test devices.

Results and Discussion

The impact ionization phenomena has been evaluated for the test devices at room temperature by using the parameter analyzer : HP-4156.

Fig.2 shows the threshold voltage as a function of the gate length of the three samples with 4, 6 and 8nm gate oxide thickness. It is indicated that the threshold voltage lowering characteristics were almost the same for three devices. The difference of threshold voltage at the long channel is simply explained by the difference of the gate oxide thickness. The threshold voltage lowering can be suppressed by the pocket implantation, and the gate length of 0.08μm becomes practical for three devices.

Fig.3 shows the substrate current characteristics as a function of the drain voltage at the gate length of 0.08μm for N-MOSFET with the gate oxide thickness of 4 and 8nm. At the low gate voltage region less than 1.0V, the substrate current of 4nm device is higher than that of 8nm device. On the contrary, in the range of higher gate voltage, the substrate

current of 8nm device is higher, due to the electric field suppression effect by the gate voltage. So called "bell shape" substrate current characteristics are observed even at drain voltage of 0.8V for 8nm device, and 0.9V for 4nm one.

The minimum drain voltage where the bell shaped substrate current can be observed (Vdmin) was estimated for 4nm and 8nm devices. Fig.4 shows Vdmin as a function of gate length. The Vdmin were decreased rapidly at the gate length less than 0.2μm for both 4nm and 8nm devices. The Vdmin at the shortest gate length of 0.08μm is 0.9V for 4nm device and 0.8V for 8nm device, while the Vdmin at the long channel is 1.15V for both devices. The calculated built-in potential (body to source barrier) of test devices is less than 0.1V, and hence it can be said that the sub-band-gap impact ionization is observed and this phenomena is enhanced by thicker gate oxide(2), (3).

The impact ionization rate (M=Isub/Id) were measured at the drain voltage of 1.5V and at the same gate over-drive for three kinds of devices (Vg=1.0V+Vt), as shown in Fig.5 (3). M is almost the same for NMOS with three different gate oxide devices at the whole gate length, which means that the impurity profiles are identical between three devices. M is constantly increased with decrease of the gate length.

Fig.6 shows M at Vd=Vg=1.2V as a function of the gate length. It is found that M is rapidly increased in the short gate length less than 0.2μm, which is consistent with a previous study(4). It is also shown that M is decreased when the gate oxide thickness is scaled down. This is because the lateral electric field is suppressed by the gate electric field and this effect is larger for thinner gate oxide at the same bias conditions. The difference of M value for three devices becomes smaller as the gate length becomes short.

The gate oxide thickness dependence of the impact ionization rate was directly estimated. Fig.7 shows the ratio of the impact ionization rate (M(8nm)/M(4nm)) as a function of the gate length. The gate oxide dependence is decreased as the gate length becomes short, and this is apparent for higher bias of 1.5V.

The lateral electric field were calculated for 0.1μm-NMOS by 3D-process/device simulator : SMART(5), as shown in Fig.8. It is found that the thinner gate oxide (4nm) suppresses the peak electric field, while enhancing the channel electric field. It implies that the non-local effect is enhanced in short channel MOSFETs (6), from Fig.7 and Fig.8.

Conclusions

In conclusion, the sub-band gap impact ionization is observed and this phenomena is enhanced for the thicker gate oxide device. Vdmin is 0.8V for 0.08μm-NMOSFET with 8nm gate oxide, while it is 1.15V at long channel. Although the scaling of the gate oxide thickness is essential for high performance MOS devices, the gate oxide thickness dependence of the impact ionization is decreased as the gate length becomes short, which indicates the non-local effect of small geometry MOSFET.

Acknowledgments

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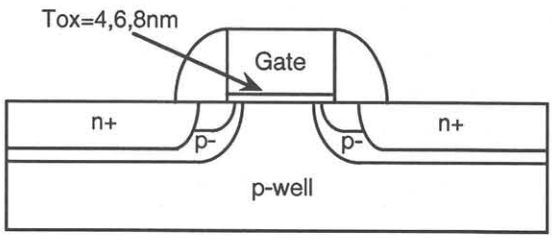

Fig.1 Cross sectional view of test devices.

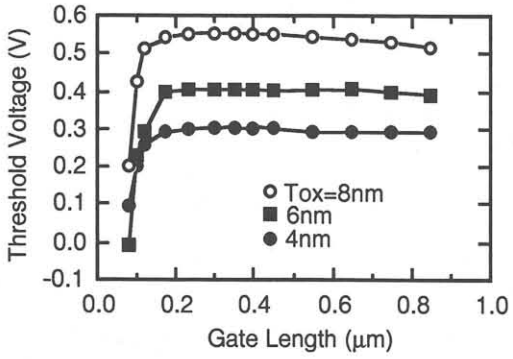

Fig.2 Threshold voltage lowering of NMOS with 4,6,8nm gate oxide.

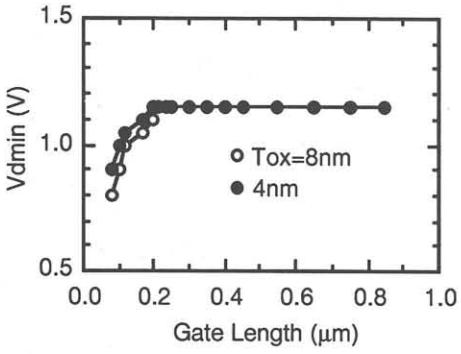

Fig.4 Minimum drain voltage where substrate current can be observed.

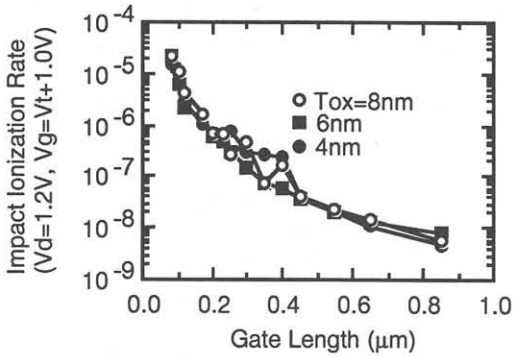

Fig.5 Impact Ionization Rate (M) at Vd=1.5V, Vg=Vt+1.0V

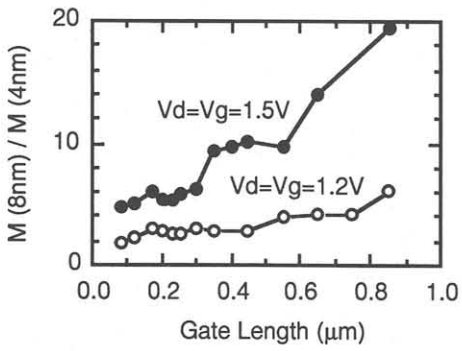

Fig.7 M (8nm) / M (4nm) as a function of gate length.

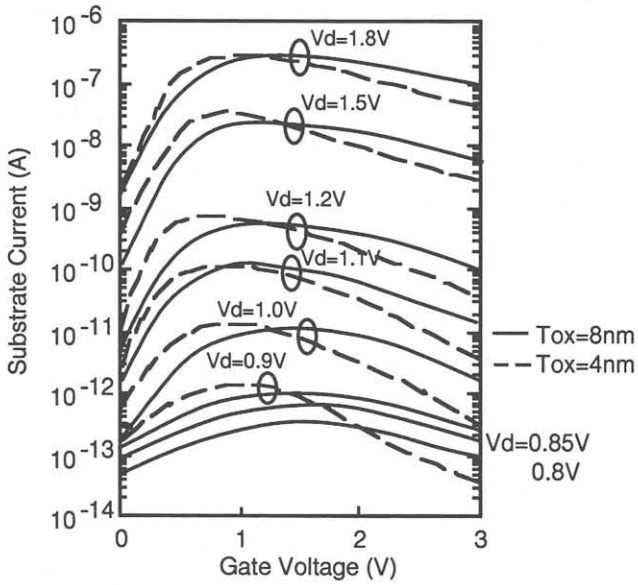

Fig.3 Substrate current characteristics for 0.08μm-NMOS with 4 and 8nm gate oxide.

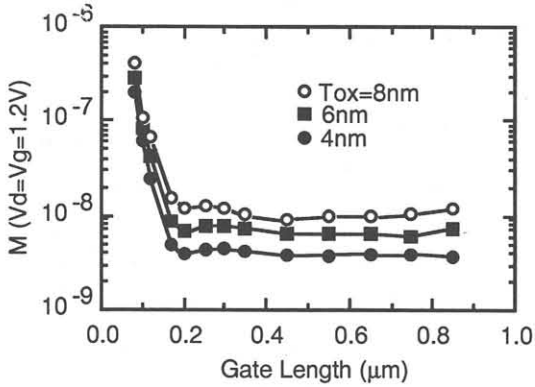

Fig.6 M as a function of gate length at Vd=Vg=1.2V

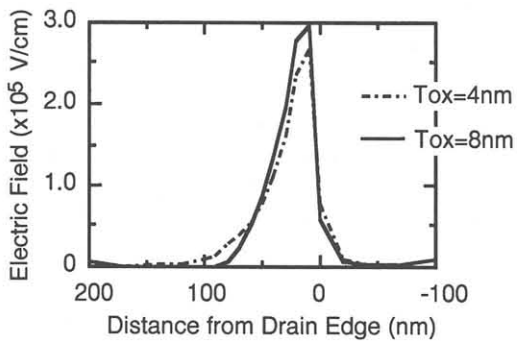

Fig.8 Lateral electric field of 0.1μm-NMOS at Vd=Vg=1.2V, simulated by SMART.