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Stress Effect on the Reliability of pMOS TFTs for 16 Mb SRAM: DC Stress at Room and Elevated Temperatures

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The electrical stress effects of pMOS TFTs used as pull-up transistors in SRAM are presented. The effect of dc stresses as occur during the standby was examined at both room and elevated substrate temperatures. The OFF regime stress leads to the drastic reduction in leakage current and concomitant increase in ON current in devices without offset. These effects are shown to be more pronounced when the stress was applied at room T rather than elevated substrate T. Also the stress induced reliability aspects of pMOS TFTs used for 4 Mb and 16 Mb SRAM are compared.

1. INTRODUCTION

The pMOS polysilicon TFTs have proven to be essential for fabricating high density SRAM circuits. With increasing memory density the dimensions of these TFTs are to be scaled down considerably. For example, the aspect ratio of TFTs has been reduced from about W / L = 0.55 / 1.2 μm for 4 Mb to about W / L = 0.36 / 0.72 μm for 16 Mb SRAM. The concern for device reliability becomes serious when its geometry is scaled down deep in submicrometer range[1].

This paper presents the observed reliability aspects of pMOS TFTs, fabricated for use as pull-up transistors in 16 Mb SRAM. During the standby, these TFTs undergo dc stresses in both ON and OFF regimes and that possibly at elevated substrate temperatures. The resulting changes of the device transfer characteristics due to these dc stress biases applied at different substrate temperatures are presented and discussed. Additionally, the stress effects of TFTs fabricated for 4 Mb and 16 Mb SRAM, respectively are compared.

2. RESULTS AND DISCUSSION

Figure 1 shows the cross-sectional view of bottom-gated pMOS TFTs with varying offsets at the drain end. The aspect ratio of the device was W / L = 0.36 / 0.72 μm and the gate oxide consisted of 20 nm - thick HTO deposited at 850 C. The maximum process temperature used after TFT fabrication was 850 C.

The transfer characteristics of TFTs without offset is presented in Fig. 2. As shown by the curve A, the leakage current, I_L measured from the virgin sample at room temperature amounts to several pA. The leakage current is shown to be enhanced by more than an order of magnitude when taken at an elevated substrate temperature of 125 C (see curve D). When the dc stress is applied for 960 s at the bias conditions, V_G = 0 V and V_D = - 6.6 V , the transfer behavior improves via reduced I_L and enhanced ON current, I_{ON}, as shown in curve B. The device characteristics further improves when V_G is moved deeper into the OFF region, i. e. V_G = 6.6 V while keeping V_D and the stress time same. In this case I_L is reduced by about two orders from the initial value, resulting in ON/OFF current ratio of 10^6. (see curve C).

Note from these measured data that the minimum I_L-value is primarily determined by the electron tunneling in the high field region near the drain. For the case of A the tunneling sets in early, assisted by the grain boundary trap states, viz. the two step tunneling processes. Also the I_L being significantly enhanced with increasing substrate temperature (curve D) clearly indicates that the tunneling is phonon-assisted [2].

The fact that I_L is drastically reduced with the application of the dc stress in the OFF regime (curve B) is a clear indication that some of the hot electrons are trapped at the interface, reducing the high field. When the gate bias is moved deeper into the OFF region more of these hot electrons should be trapped in the oxide, further reducing the field, hence I_L (see curve C).

To examine the lifetime of these trapped electrons the data was taken again from the sample for C after two months and is presented in curve C'. The leakage level in C' is shown to be slightly larger than that in C but still is smaller than the initial value by orders of magnitude. This suggests that the electrons are trapped semi-permanently and only a mere fraction has been released during the elapsed time.

Figure 3 shows the same set of data as in Fig. 2, measured however from TFTs with 0.4 μm offset. In this case I_L from the virgin sample at room temperature is observed to remain below 0.1 pA level. Also the same dc stress as in Fig. 2 does not give rise to significant changes in transfer curves. This can be expected, since with the offset the field near the drain is considerably reduced and the tunneling does not become appreciable at room temperature.

Figure 4 summarizes the stress-induced effects. Here V_D was fixed at -6.6 V, while V_G was varied from -10 V to +10 V. In the case of no offset, the ON regime stress

($V_G < 0$) slightly reduces I_L, while I_{ON} remains practically unchanged. Due to OFF regime stress ($V_G > 0$), I_L is drastically reduced and I_{ON} is increased appreciably. This is consistent with the model of electrons being trapped in the oxide, as dictated by the bias voltages used. With offset of 0.4 μm the transfer characteristics are practically unchanged for all stress biases examined, as expected from the previous discussions[3].

Figure 5 shows the effects of dc stress as influenced by varying substrate temperatures. Specifically the modification in the transfer curves due to stress at both room and elevated substrate temperatures was measured and presented in Fig. 5. It is emphasized here that the degree of I_L-reduction and I_{ON}-enhancement due to OFF regime stress at an elevated T (125 C) is smaller than that corresponding to the room temperature stress. This finding, reported here for the first time, is novel, especially in view of the fact that I_L at high T is increased by orders of magnitude due to phonon-enhanced electron tunneling (curve D in Figs. 2, 3). However this observation is entirely consistent with the aforementioned model of trapped electrons. With increasing T the quasi-Fermi level moves toward the midgap and the amount of electrons trapped at the interface traps should therefore decrease[4].

Figure 6 shows the stress induced shift in the voltage, V_{min} at which the minimum I_L is observed to occur. This shift which reflects roughly the corresponding shift in V_{TH} is seen to be substantial without offset, however negligeable with offset.

In Fig. 7 the transfer curves are presented from TFTs fabricated for both 4 Mb and 16 Mb SRAM applications. The device parameters are: W / L = 0.55 / 1.2 μm and the gate oxide thickness of 30 nm for the case of former and W / L = 0.55 / 0.72 μm and oxide thickness of 20 nm for latter. In both cases the incorporation of 0.4 μm offset gives rise to drastic reduction of I_L to possibly the generation limited level at a relatively small expense of I_{ON} decrease.

The stress effects of these two kinds of devices without offset are shown in Fig. 8. Here the dc biases used are V_G = 0 V for both cases and V_D = - 10 V for 4 Mb and V_D = - 6.6 V for 16 Mb SRAM TFTs. These biases roughly simulate the standby condition except that the drain voltages chosen are twice the respective supply voltage. It can be clearly noted from these data that the overall effect of stress is smaller for the case of TFTs for 16 Mb SRAM. Although the device in this case has shorter channel length and is therefore more prone to hot carrier induced effect, the smaller supply voltage used more than offsets the overall stress induced changes in the transfer curve.

3. CONCLUSIONS

The striking features of electrically stressing pMOS TFTs are as follows: (1) The effect is most pronounced in devices without offset, (2) dc stress in the OFF regime results in drastic reduction of I_L, and the the degree of I_L-reduction is more apparent for the case of room temperature stress rather than that at elevated substrate temperatures. These findings can be interpreted in terms of hot electrons being trapped in the oxide. The lifetime of these trapped electrons are observed to be nearly permanent.

An incorporation of proper offset enables to meet the specifications required for active loads in SRAM and also renders the device performance stable against the dc stress. Even for the case of device geometry deep in submicrometer range the offset is still very effective for realizing the desired transfer curves. Additionally the relative effect of dc stress becomes small in smaller geometry devices. This is due to smaller supply voltage more than compensating enhanced hot carrier effect in shorter channel devices.

References

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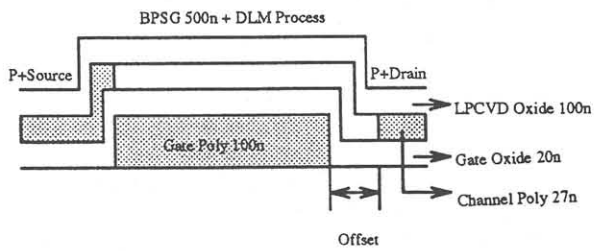

Fig. 1 Cross-sectional view of pMOS TFTs.

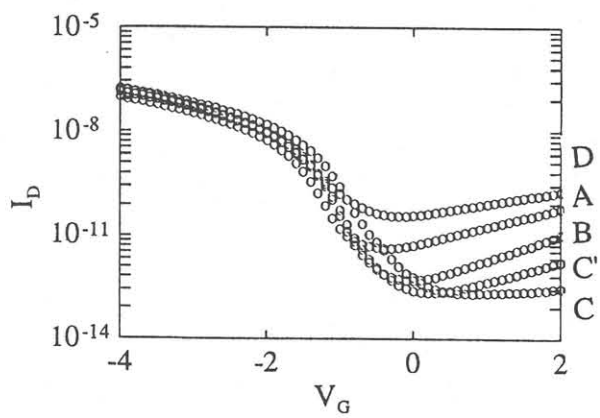

Fig. 2 I_D vs. V_G in pMOS TFT with W / L = 0.36 / 0.72 μm and no offset; A is for initial data before stress; B after stress at V_G = 0 V, V_D = - 6.6 V for 960 s; C after stress at V_G = 6.6 V, V_D = - 6.6 V for 960 s; C' the C-data taken after two months; D initial data before stress taken at substrate temperature of 125 C.

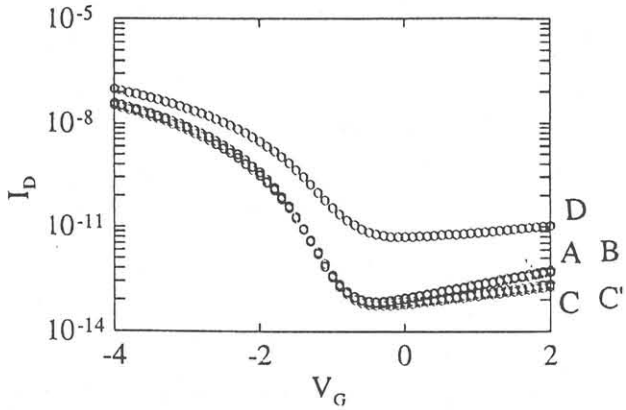

Fig 3 Identical set of data as in Fig. 2 from TFT with an offset of 0.4 μm.

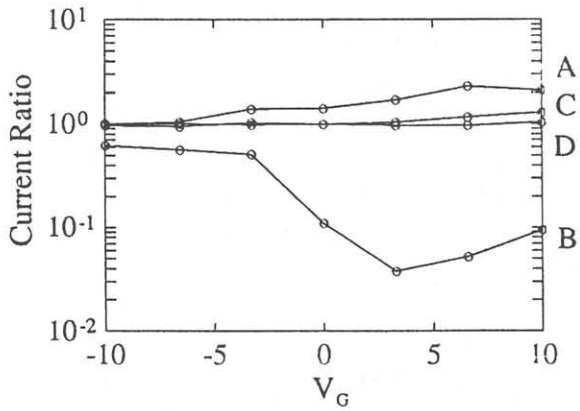

Fig. 4 The ON and OFF currents taken after dc stress and scaled with respective initial values vs. gate stress voltage. With V_D fixed at -6.6 V the stress time was 960 s for each V_G. The curves A, B are for the scaled ON and OFF currents without offset; C, D with offset of 0.4 μm.

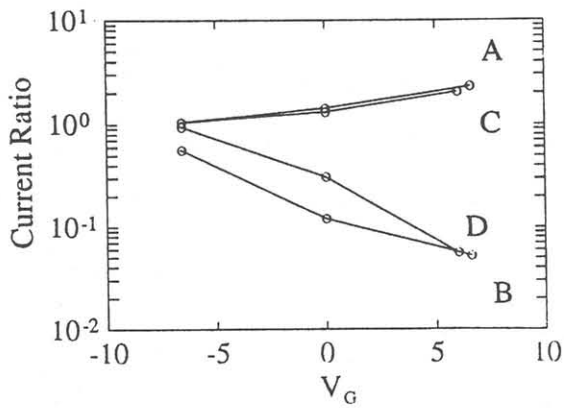

Fig. 5 The ON and OFF currents taken after dc stress and scaled with respective initial values vs. gate stress voltage. With V_D fixed at -6.6 V stress time was 960 s for each V_G. The curves A, B are for the scaled ON and OFF currents with stress applied at room T; C, D at 125 C.

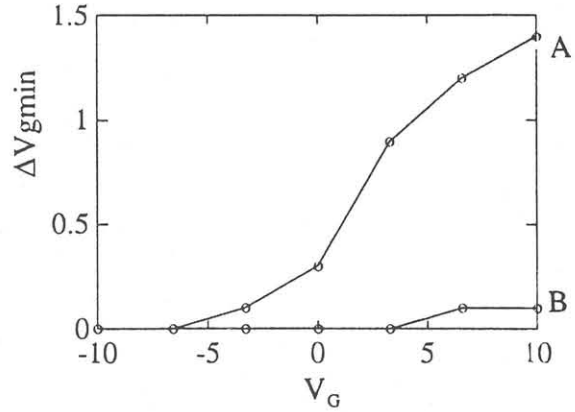

Fig. 6 Shift in V_{min} at which I_L-minimum occurs vs. gate stress voltage. With V_D fixed at -6.6 V the stress time was 960 s: the curve A is for device without offset; B for the 0.4 μm offset.

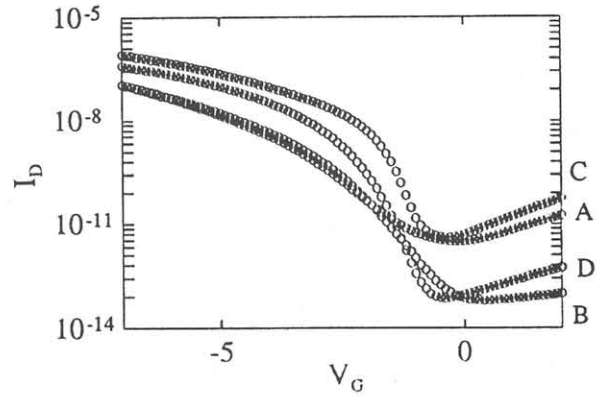

Fig. 7 The transfer curves from TFTs fabricated for 4 Mb and 16 Mb SRAM. The curves A, B are from the former device with W / L = 0.55 / 1.2 μm and the oxide thickness of 30 nm with and without offset of 0.4 μm, respectively: the curves C, D are for the latter device with 0.36 / 0.72 μm and oxide thickness of 20 nm.

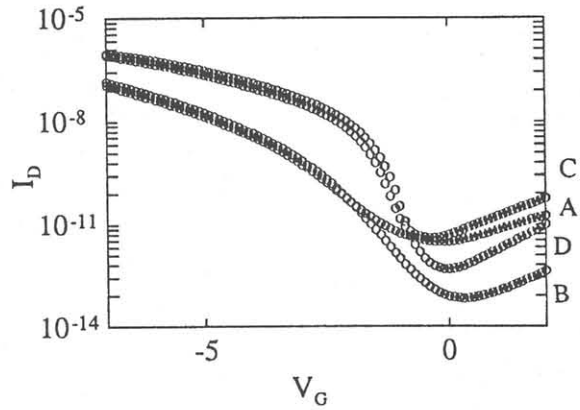

Fig. 8 The transfer curves from TFTs fabricated without offset for 4 Mb and 16 Mb SRAM. The curves A, B are from the former device before and after the stress: C, D are from the latter before and after the stress. The device parameters are same as in Fig. 7 and the stress conditions are: V_G = 0 V and V_D = - 10 V for the former and V_D = - 6.6 V for the latter for 960 s.