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Development of Sub-Quarter-μm MONOS Type Memory Transistor

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A MONOS (metal/oxide/nitride/oxide/semiconductor) type nonvolatile memory transistor with 0.23 μm gate length has been developed. The memory transistor offers high endurance, low programming voltages and the distribution of programmed threshold voltages is very small, allowing low read out voltage. By introduction of a rapid thermal nitridation (RTN) step into the fabrication of the ONO (oxide/nitride/oxide) layer an enhancement in erase speed of one decade is achieved. The RTN furthermore improves oxidation resistance of the nitride layer, so that thinner ONO layers will be feasible.

1. Introduction

The MONOS (metal/oxide/nitride/oxide/semiconductor) memory device (fig. 1) has been proposed as a small size, low power nonvolatile memory device[1,3]. In this study we show the applicability of MONOS memory devices to sub-quarter-μm gate lengths of 0.23 μm with an oxide-equivalent dielectric thickness of about 11 nm.

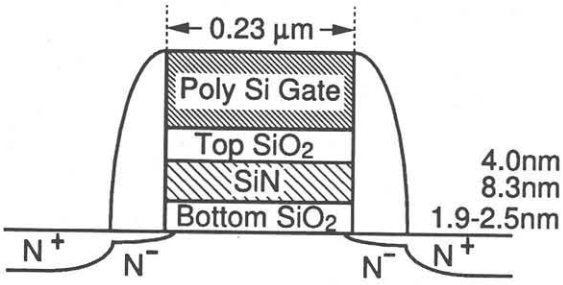

Figure 1: Schematic cross-section of MONOS memory transistor.

Moreover, the introduction of a rapid thermal nitridation (RTN) step into the fabrication of ONO (oxide/-nitride/oxide) layer of MONOS transistors is investigated. The key point for future MONOS devices with shorter gate lengths for low power applications will be the scaling of the ONO layer. A relatively thick bottom oxide layer is needed to ensure a 10 year data retention, which on the other hand reduces the erase speed. Also, a minimum nitride layer is required to avoid oxygen penetration through the nitride layer during top oxide fabrication. It was found by investigation on MONOS capacitors that the oxidation resistance can be improved by pre-treatment with RTN prior to Si_3N_4 low pressure chemical vapor deposition (LPCVD)[2]. This previous result is confirmed by recent investigations carried out on ONO layers (fig. 2).

2. Process

Samples are fabricated on p-type silicon substrates. After LOCOS isolation, the gate dielectric consisting of an oxide/nitride/oxide layer is formed as follows. A tunnel oxide of 1.9 to 2.5 nm is formed by nitrogen diluted oxidation, the aforementioned RTN step is then applied

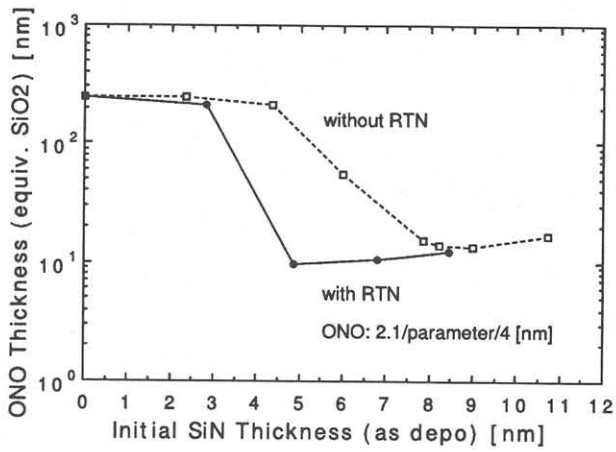

Figure 2: ONO thickness equivalent SiO_2 after top oxide formation versus initial Si_3N_4 thickness shows improved oxidation resistance by RTN pre-treatment below initial Si_3N_4 thickness of 8 nm.

at 1000°C for 1 min in an NH_3 atmosphere. This is followed by LPCVD of 10.5 nm Si_3N_4 at 680°C. Deposition times of Si_3N_4 LPCVD are adjusted to account for the different incubation times of samples with and without RTN pre-treatment. The initial nitride thickness is reduced during the pyrogenic top oxidation step, leaving an 8.3 nm nitride layer and creating 4 nm thick oxide on the Si_3N_4. Gate patterns are formed by lithography and resist thinning method. Fabrication is completed by source/drain formation, interlayer deposition and contact/electrode formation. The schematic cross-section of the MONOS transistor is shown in figure 1.

3. Results

Measured results of the gate length dependency of initial threshold voltages V_{th} of enhancement type short channel MONOS transistors are shown in figure 3. A transistor with 0.23 μm gate length and 10 μm gate width is chosen for the following measurements.

Write/erase characteristics of a sample with 2.2 nm bottom oxide, treated with RTN are shown in figure 4 for write and erase programming voltages V_{pw} and V_{pe} ranging from ± 5 to ± 10 V.

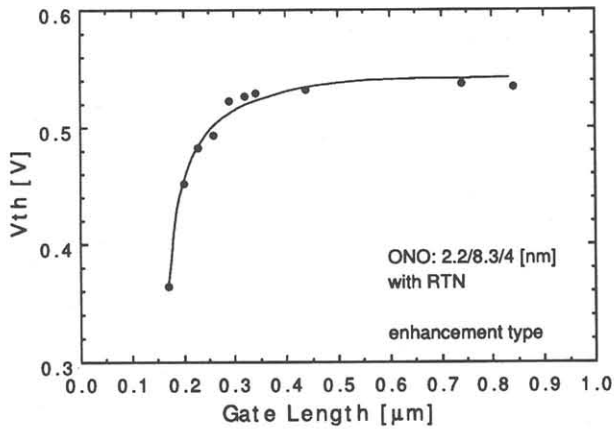

Figure 3: Gate length dependency of initial threshold voltages of enhancement type short channel MONOS memory transistors.

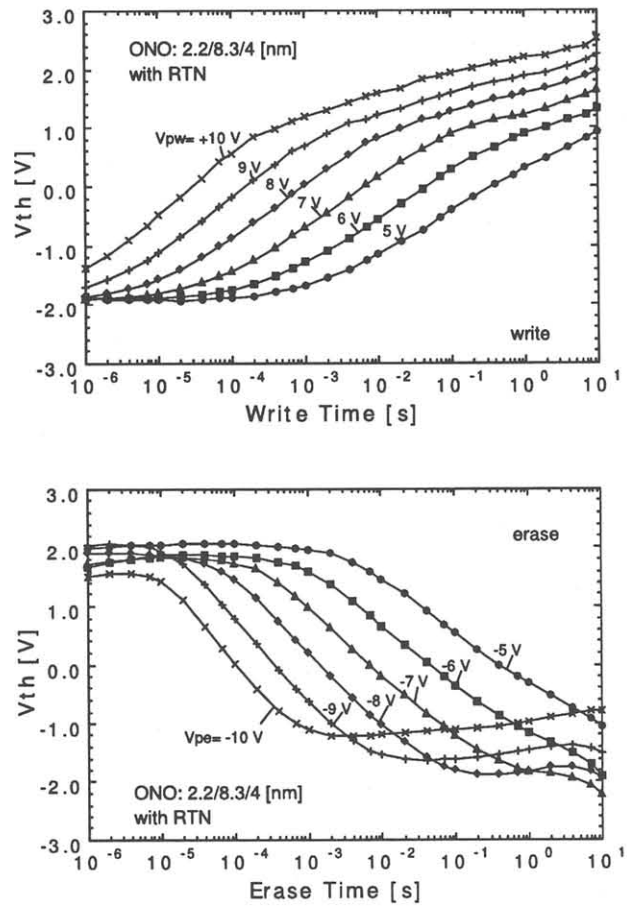

Figure 4: Write/erase characteristics for a range of write/erase programming voltages V_{pw} and V_{pe} between ±5 and ±10 V, in 1 V steps.

Erasing of the cell fabricated with RTN pre-treatment can be achieved as fast as a conventional MONOS transistor with 0.6 nm thinner bottom oxide (fig. 5). A difference in bottom oxide thickness of 0.3 nm is equivalent to a difference in erase speed of about one decade, with write speed being independent of the bottom oxide thickness.

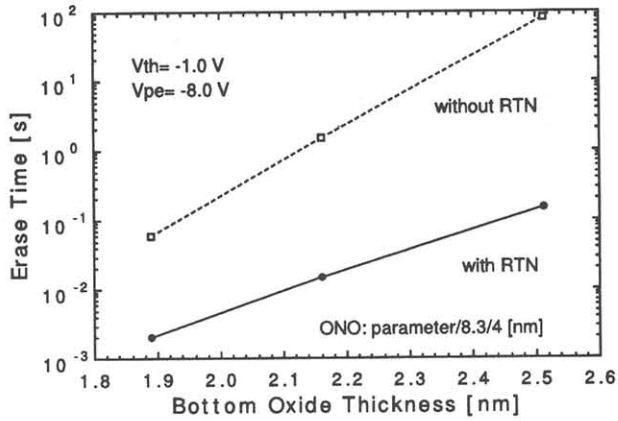

Figure 5: Dependency of erase time needed to erase to V_{th}=-1.0 V with V_{pe}=-8.0 V on bottom oxide thickness (oxide thickness before RTN and/or LPCVD).

Results of write/erase decay rates of an RTN treated cell show retention characteristics of the level of a conventional cell having about 0.3 nm thinner bottom oxide (fig. 6). Therefore, the improvement in erase speed and weakening of retention characteristics by the introduction of RTN indicate a gain which is equivalent to a 0.3 nm reduction of the bottom oxide thickness.

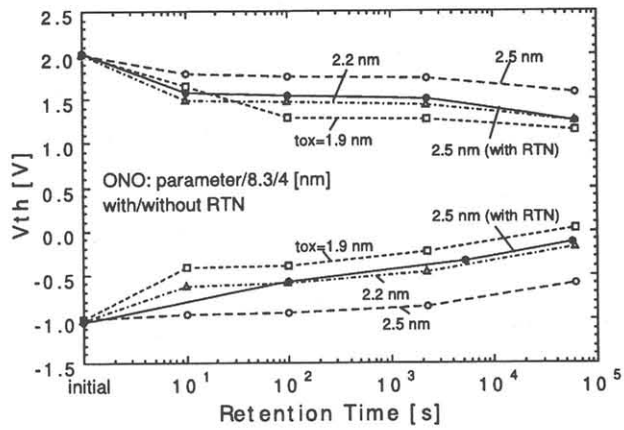

Figure 6: Comparison of data retention for initial threshold voltages of V_{thw}=2.0 V and V_{the}=-1.0 V for varying bottom oxide thickness with and without RTN pre-treatment.

Measurements of data retention characteristics prove 10 year retention at 85°C for the conditions of writing with V_{pw}=10 V, 10 ms and erasing with V_{pe}=-8.0 V, 100 ms (fig. 7).

The difference between maximum and minimum V_{th} in the written and erased states without verify over 33

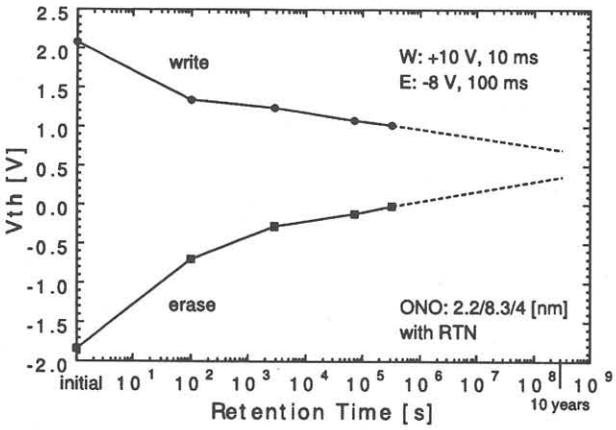

Figure 7: Data retention at 85°C ensuring 10 year retention. For write with 10 V, 10 ms and erase with -8V, 100 ms a V_{th} window of 0.3 V remains after 10 years at 85°C.

transistors is just 0.2 V, which is very small compared to other type memories[4] (fig. 8).

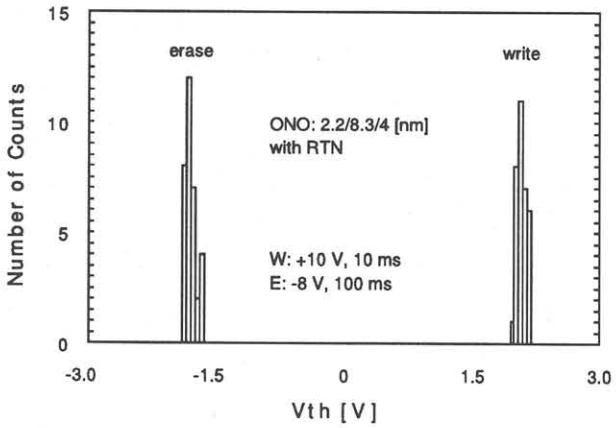

Figure 8: V_{th} distribution over 33 transistors of only 0.2 V of MONOS memory cell after write/erase without verify.

Endurance characteristics prove device applicability to at least 1 million write/erase cycles (fig. 9).

4. Conclusion

A MONOS memory transistor with a gate length of only 0.23 μm has been developed. The memory offers high memory endurance and the threshold voltage V_{th} distribution of MONOS transistors is very small, allowing low read out voltage. Programming voltages are lower than those for floating gate devices. By introduction of an RTN step into the fabrication of the ONO layer an improvement in erase speed has been achieved. Compared to a conventional type device without RTN which ensures the same data retention, a gain in erase speed of 1 decade is achieved (same as for a 0.3 nm thinner oxide without RTN). The RTN step furthermore improves the oxidation resistance of the Si_3N_4 layer, so that scaling to smaller gate lengths and thinner ONO layers will be possible, resulting in a reduction of the applied pro-

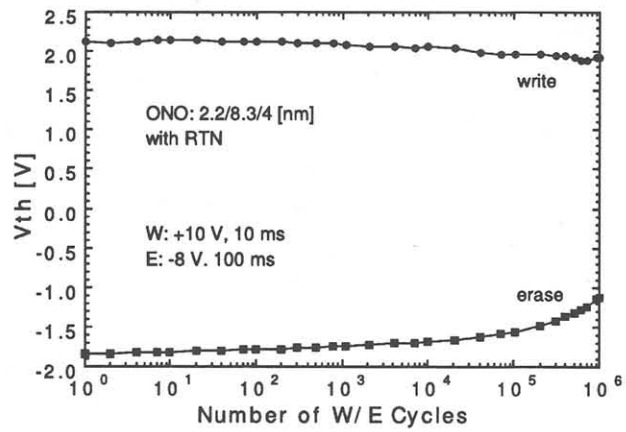

Figure 9: Endurance characteristics up to 1 million write/erase cycles.

gramming voltages V_{pw} and V_{pe}. The MONOS memory has potential for application to low programming voltages and offers small V_{th} distribution without verify and high memory endurance.

The scalability of the MONOS device to gate lengths below 0.23 μm with thinner and optimized ONO layers makes the MONOS memory a very promising memory device for future low power high density applications.

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References

1) E. Suzuki, Y. Hayashi, K. Ishii, H. Hiraishi: Jpn. J. Appl. Phys. **22** (1983), Suppl. 22-1, 581.
2) T. Böhm, A. Nakamura, M. Kubota, M. Yamagishi: Extended Abstracts (The 41st Spring Meeting, 1994), The Japan Society of Applied Physics, 28p-ZW-7, 663.
3) M. Yamagishi, A. Nakamura, H. Aozasa, T. Boehm, M. Kubota: Proceedings of the 47th Symposium on Semiconductors and Integrated Circuits Technology, Tokyo December 8, 9 (1994), 114.
4) A. Nakamura, T. Böhm, H. Aozasa, M. Yamagishi: Extended Abstracts (The 42nd Spring Meeting, 1995), The Japan Society of Applied Physics, 30p-R-4, 827.