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A High Pressure High Temperature Poly Buffer LOCOS (HP-HTPBL) Isolation Process for 1Gbit Density Non Volatile Memories.

S.DELEONIBUS, F. MARTIN, S.S.KIM(*), A.EMAMI(*), B.FLORIN, M. HEITZMANN and C. LEROUX

LETI(CEA) Dept de Microélectronique - CENG 17 Avenue des Martyrs 38054 Grenoble Cedex 9 France
(*) GASONICS International, 2730 Junction Avenue, San José(CA) USA

The characterization of High Pressure High Temperature Poly Buffer LOCOS (HP-HTPBL) isolation for 0.2µm design rules Non Volatile memories of the 1Gbit generation is presented. Reduced bird's beak and improved gate oxide defect density, QBD and low junction leakage are obtained by combining High Pressure Oxidation and High ramp up and down temperature rates. A compatibilty with 200 mm wafers processing is demonstrated. 0.2µm design rules active and field isolation devices for Non Volatile Memories are achieved.

1. INTRODUCTION

The field oxide thinning of conventional or improved LOCOS isolations is particularly critical on Non Volatile memories devices because of the high programming voltage constraints combined with high performance devices optimization. Several attempts have been made to avoid this problem by using trench isolation[1),2)] or minimize it by using 1100°C high temperature Poly Buffer LOCOS[3)]. At this temperature, high pressure oxidation also improves the oxide thinning in small isolation spaces[4)].

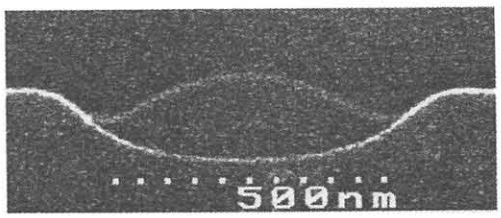
The HP-HTPBL process has been developped to combine the advantages of high temperature and high pressure on the reduction of field oxide thinning as well as thermal budget (reduction of oxidation time) at 1100°C. A vertical High Pressure Oxidation furnace from GASONICS has been used: the oxidation pressure was as high as 25 atmospheres, ramping up and down rates were as high as 30°C/min. and 12°C/min. respectively[5)].

2. DIMENSIONAL LOSS

Cross sections of the HP-HTPBL structure are shown in figures 1a and b for a 4000Å as grown 1100°C steam oxidation under 25 atmospheres: a) 0.5 µm spacings; b) 0.20µm finished wide diffusion resulting in a 0.08µm bird's beak. The patterning and etching process have already been described[3)].

The reduction of the linear part of the oxidation kinetics with increasing temperature will favourably impact the reduction of bird's beak in the High Pressure Oxidation regime[4)] as compared to the 1 atmosphere results: figure2 confirms this behaviour on statistically measured ΔWeff from narrow active devices transconductance. The reduction is also visible for lower field oxide thickness.

(1a)



(1b)

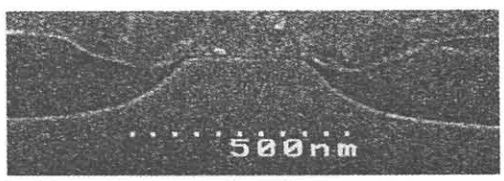


Figure 1 HP-HTPBL morphology. Oxidation pressure 25 atm. Oxidation temperature 1100°C. Field oxide 400 nm as grown Cross sections of: (a)0.50 µm spacings b) 0.20 µm active area

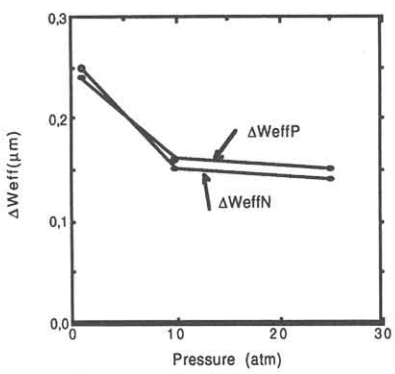


Figure 2 HP-HTPBL process. ΔWeff as a function of pressure. Oxidation temperature 1100°C.

3. ACTIVE DEVICES CHARACTERISTICS

Subthreshold Ids(Vgs) characteristics of N and P narrow channel active transistors confirm the reduction of bird's beak as compared to atmospheric pressure

samples(figures 3a and b): reduced narrow channel and lower body effects are obtained by increasing the oxidation pressure. PMOS devices are mostly improved because of the reduced pile up of the diffused N-Well Phosphorous at the channel edge. No subthreshold hump is observed on the characteristics for both N and P channel devices even for polarized bulk.

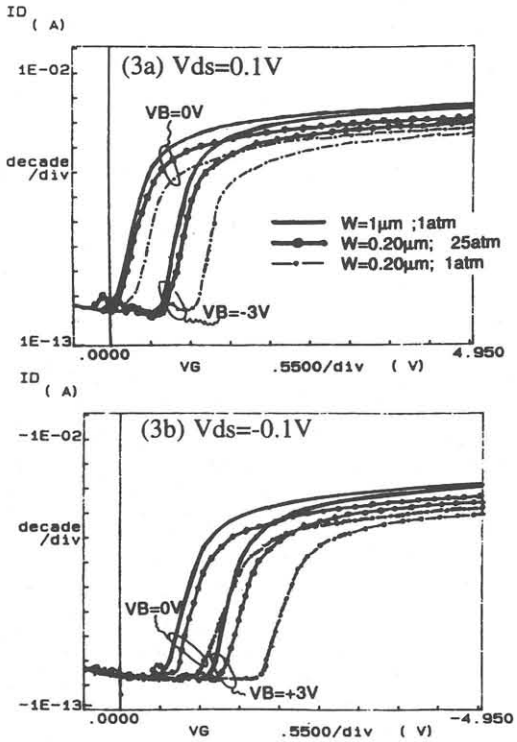


Figure 3 HP-HTPBL process. Subthreshold Id(Vgs) characteristics of L=1µm and W =0.20 &1 µm MOS transistors at different VB values for: (a) N channel (b) P channel devices. Field oxidation 400 nm 1100°C. Different oxidation pressures

4. GATE OXIDE QUALITY

Improved gate oxide defect density and Qbd can be obtained by increasing oxidation pressure or ramping up rates to 30°C/min. and ramping down rates to 12°C/min.: figures 4 and 5 show the cumulative failures of breakdown field and Qbd respectively on 12m active area perimeter capacitors. These behaviours are explained by reduced lateral stress brought by High Pressure (up to 25atm) High Temperature(1100°C) oxidation. In all cases, the gate oxide intrinsic breakdown is 15MV/cm.

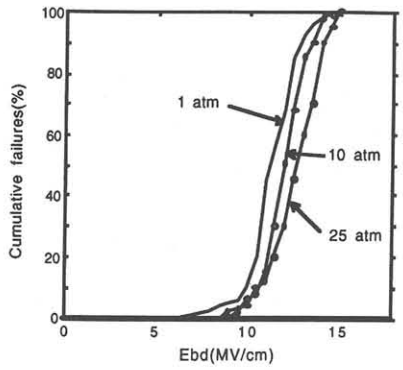


Figure 4 HP-HTPBL process. Cumulative failures of breakdown field for 7 nm gate oxide for 10 atm, 25 atm field oxidationat 1100°C. Ramping up : 30°C/min. Ramping down: 12°C/min. Reference 1 atm 1100°C 10°C/min. Perimeter: 12m. Sampling: 210 capacitors/split

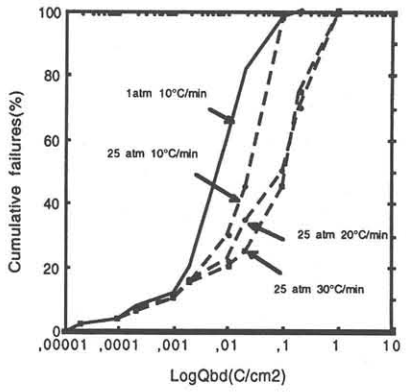


Figure 5 HP-HTPBL process. Cumulative failures of 7 nm gate oxide Qbd. Field oxidation: 25 atm steam 1100°C. Ramping up rates: 10, 20 and 30°C/min. Perimeter: 12m. Sampling: 210 capacitors/split

The Qbd results have been correlated to medium range(300 nm) roughness which is 50% larger in the 1 atm reference case than in the 25 atm oxidation 30°C/min ramp up case as the AFM results can show(figure 6). Due to the shorter process time in the 25 atm,30°C/min case, the recristallization of the buffer a-Si will be more homogeneous and oxygen diffusion at the grain boundaries will be minimized compared to a conventionnal reference process.

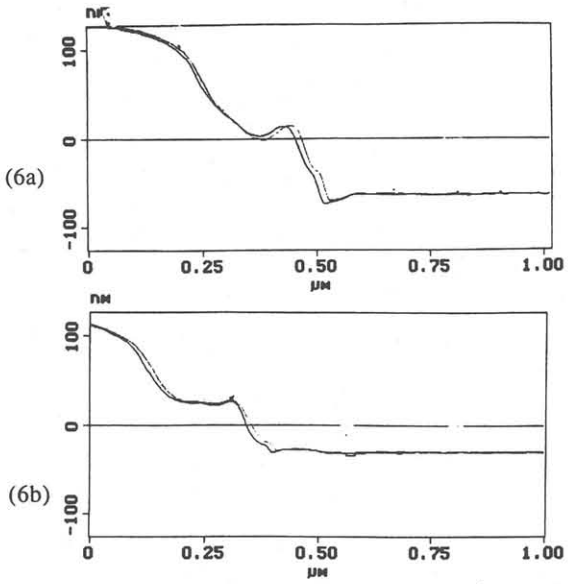


Figure 6 AFM profile of medium range roughness at the field oxide(active area step. Different points 300nm distant. 1100°C 500 nm field oxidation (a) 1 atm,10°C/min ramp-up (b) 25 atm, 30°C/min ramp-up

5. 200mm WAFERS DEFORMATIONS

The use of High Pressure can allow high ramping up and down rates to minimize 8 inches wafers warpage (figure 7). Under these extreme conditions the junction leakage measured on 12 m perimeter active area diodes is less than 5pA/cm at 5V which is comparable to atmospheric pressure results

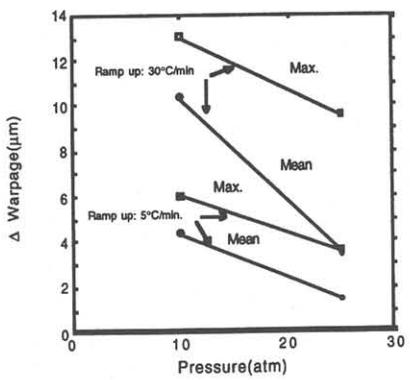


Figure 7 Warpage variations on 8 inches diameter wafers for 5°C/min. and 30°C/min. ramping up rates. HP-HTPBL process. 700nm steam oxidation at 1100°C under 10 and 25atm Sampling: 600 sites/wafer

6. FIELD ISOLATION. BORON O.E.D..

Field isolation can be ensured down to 0.5µm (n+/n+) or 0.55µm(p+/p+) of diffusion/diffusion distance(figure 8): the poly gate devices isolation is limited by GIDL[3] and metal gate devices punch-through is avalanche breakdown controlled by VT implant optimization at 12V in p-Well and -12V in N-Well (Vd=Vg condition for a leakage of 10pA/µm of a 2000µm device width)

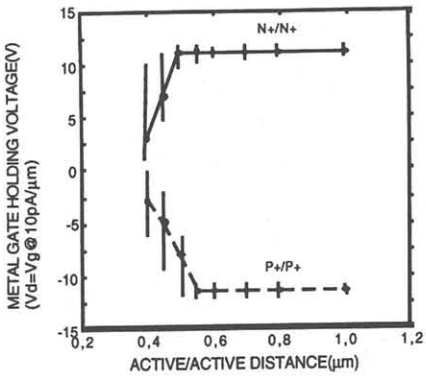


Figure 8 HP-HTPBL process. Metal gate field transistors devices isolation (Vd=Vg for 10pA/µm leakage). 400 nm as grown field oxide 1100°C 25 atm

Reduced thermal budget can be achieved at 1100°C and will ease the use of thin p/p+ epi substrate to achieve controllable isolation between wells: the masked and Oxidation Enhanced Diffusion(OED) of Boron are reduced by using high pressure oxidation as compared to atmospheric pressure oxidation(figure 9). The p+ buried layer to p+ drain, the 0.60 µm p-Well/p+, the 0.30µm N-Well/n+ drain DMOS devices metal gate devices isolation are punchthrough free. Latch-up control is eased by using 25 atmospheres oxidation as compared to the 1 atmosphere case and decreases the dispersion of the p+/N-Well/P-Well/n+ field devices holding voltage

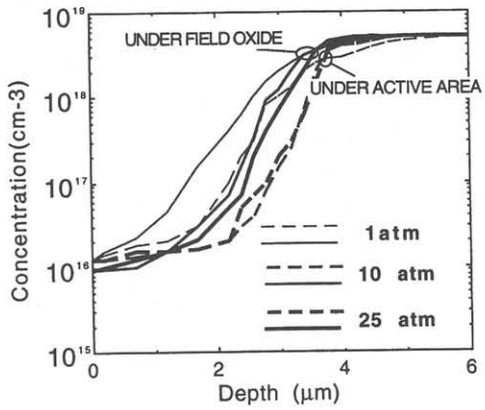


Figure 9 HP-HTPBL process. Spreading resistance profile of 4µm epi p/p+ wafers for 500 nm oxidation at 1100°C for 1, 10 and 25 atm steam pressure. Ramping up 10°C/min. Dashed lines : nitride masked diffusion. Solid lines: OED.

7.REFERENCES

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