A Novel Planarization of Trench Isolation Using a Polysilicon Layer As a Self-Aligned Mask

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Abstract

The planarization of oxide-filled trench isolation has been investigated. Results show that the planarization by the CMP-only process results in dishing effect in wide field regions. It has nonuniform polish and is difficult to control. On the other hand, excellent uniformity and surface planarity can be achieved by using a combination of a polysilicon layer as a self-aligned mask and CMP processes. This process is a very promising candidate for oxide-filled trench isolation.

Introduction

To achieve the scaled, high-density, and high-performance ULSI devices and circuits, the oxide-filled trench isolation is the most promising option [1~2]. Therefore, the etchback and planarization of oxide-filled shallow trenches becomes a key processing step. The conventional resist planarization and RIE etch back process has cumulative tolerences associated with large film thickness and easily result in final non-planarity surface [3]. A chemical-mechanical polishing (CMP) process has been proposed to achieve the planarization of silicon surface [4~5]. However, a CMP-only process has nonuniform polish and is difficult to control. It results in dishing effect in wide field regions. A combination of dry etch and CMP process, with an extra mask to reduce dishing effects in wide field regions, has been proposed to achieve excellent uniformity [3].

In this work, we present a novel planarization technique using a combination of self-aligned polysilicon layer over the field regions and CMP processes to achieve excellent uniformity and reduce the dishing effect in wide field regions.

Experiments

The process (self-align + CMP) sequence is shown in Fig. 1. A complete structure of oxide-filled trenches is shown in Fig. 1(a). First, the trench hard mask was fabricated that consisted of 20 nm of thermally grown pad oxide and 120 nm of SiN. The hard mask was etch first by RIE and then silicon trench (550 nm) was performed in a Cl_2 / O_2 plasma. After the removal of photo resist, wafers were cleaned. A 30 nm thick silicon dioxide was grown in an O_2 ambient at 925°C. Next, 900 nm thick LPCVD oxide was deposited to refill the shallow trenches. Then, a 300 nm thick LPCVD polysilicon layer was deposited.

The polysilicon layer was first polished at 4 psi with a dilute 3:1 slurry A listed in Table 1 until the polysilicon layer on the active regions was removed. However, the field regions were still capped by a polysilicon layer as shown in Fig. 1(b). The oxide refill on active regions was then dipped to the level of field oxide with a buffer hydrofluoride acid. Next, the rest of polysilicon layer was polished at 4 psi with a dilute 3:1 slurry A. The oxide refill then underwent polishing only for a short time (45 sec) at 7 psi with a dilute 2:1 slurry B listed in Table 1 as shown in Fig. 1(c). The CMP process was followed by the RIE etchback. The RIE etchback process was stopped until the SiN layer remained 50~60 nm. After the RIE process, the wafers were cleaned and then annealed in a N_2 ambient at 900°C for 30 min. The remained nitride and pad oxide were then removed by wet etching as shown in Fig. 1(d).

Results and Discussion

Fig. 2(a) and 2(b) show the removal rates of polysilicon, CVD oxide, and SiN with pressures of 4 psi and 7 psi. The various ratios of water/slurry A and water/slurry B were used as shown in Fig. 2(a) and 2(b),

respectively. The removal rate of polysilicon reaches 405 nm/min at 4 psi with a dilute 3:1 slurry A. The removal rate of CVD oxide is only 4.5 nm/min at 4 psi with the same slurry. The reason is that the strength of Si-Si bond is weaker than that of Si-O bond. Therefore, the chemical removal rate of polysilicon becomes a critical component of the removal process. However, the chemical removal rate of oxide has little influence on the removal process. The removal rates of CVD oxide and SiN reaches 116 nm/min and 50.5 nm/min, respectively, at 7 psi with a dilute 2:1 slurry B as shown in Fig. 2(b). The etch selectivity of polysilicon with respect to CVD oxide reaches 93 at 4 psi with a dilute 3:1 slurry A as shown in Fig. 3(a). Therefore, the process (b) has little influence on oxide thickness. However, the etch selectivity of CVD oxide to SiN as shown in Fig. 3(b) is only 2~3 at 7 psi with a dilute 2:1 slurry B. Hence, the CMP-only process suffers from the problem of controllability. Fig. 4(a) shows the CMP-only process results in dishing effect in wide field regions (500 μm), while, Fig. 4(b) shows the process considered in this work (self-align + CMP) can achieve fully planar surface. Fig. 5 shows dishing results using CMP-only process and self-align + CMP process. Obviously, the self-align+CMP process can improve the planarization of trench isolation with variable size and pattern factor. Fig. 6 shows the deviation during polish and the difference in oxide thickness associated with cumulative polish time in a blanket wafer which a 900 nm thick CVD oxide was deposited on it. It reveals that the self-align + CMP process undergoing short-time (45 sec) polish on oxide can achieve better uniformity (5%) than the CMP-only process (15%) undergoing long-time polish (8 min).

Conclusions

An excellent planarization of oxide-filled shallow trenches has been demonstrated successfully. This process uses a combination of a polysilicon layer as a self-aligned mask and CMP processes. With this process, the planarization of excellent uniformity can be achieved. Therefore, this is a very promising process for trench isolation.

References

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Table 1

	slurry A	slurry B
PH	11.0~11.5	10.0~10.3
particle size (nm)	70~90	30
Wt. % solids	28	30
Viscosity (cps)	< 25	< 150

(a)
poly-Si
TEOS
SiN
SiO₂

(b) 1st CMP (slurry A)

(c) wet etching (BOE) + 2nd CMP (slurry A, slurry B)
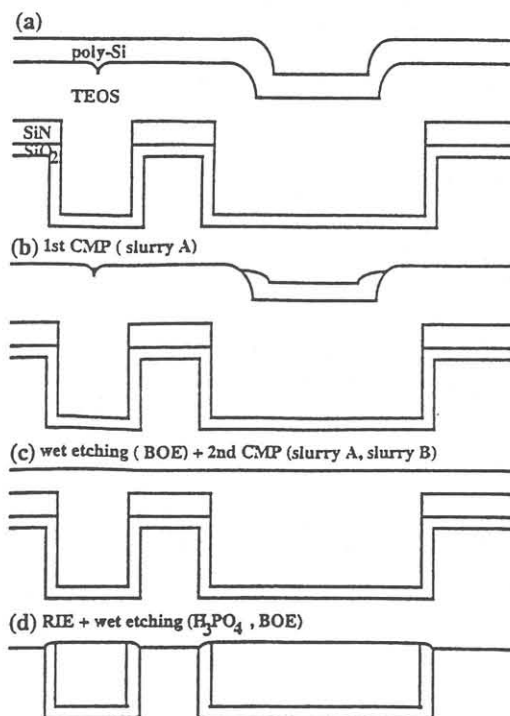
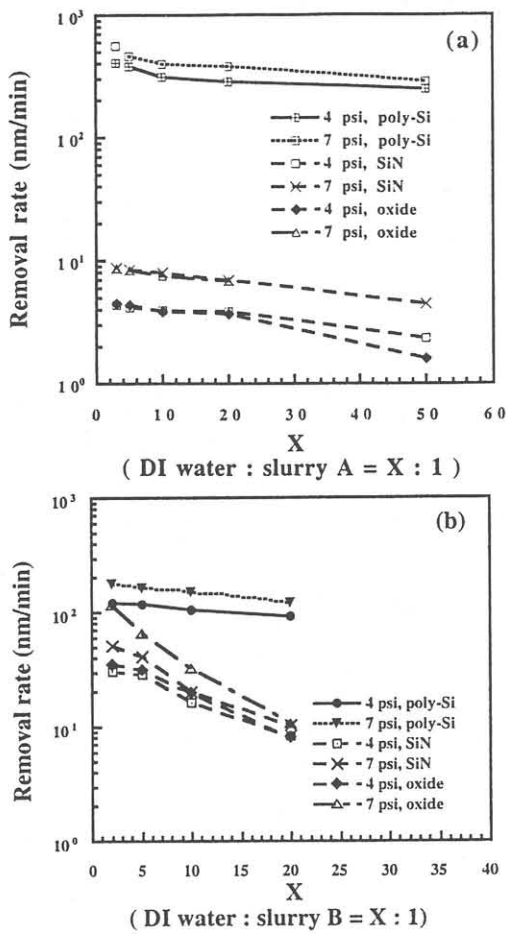(d) RIE + wet etching (H₃PO₄ , BOE)

Fig. 1. The process sequence.

Fig. 2. The removal rates of poly-Si, oxide, and SiN with slurries (a) slurry A (b) slurry B.
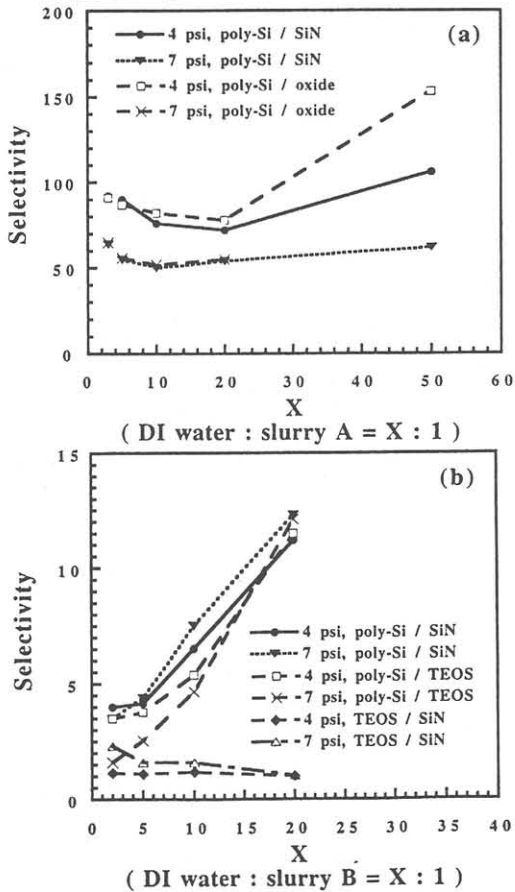

Fig. 3. The etch selectivity (a) poly-Si to oxide and SiN (slurry A) (b) poly-Si to oxide and SiN, and oxide to SiN (slurry B).
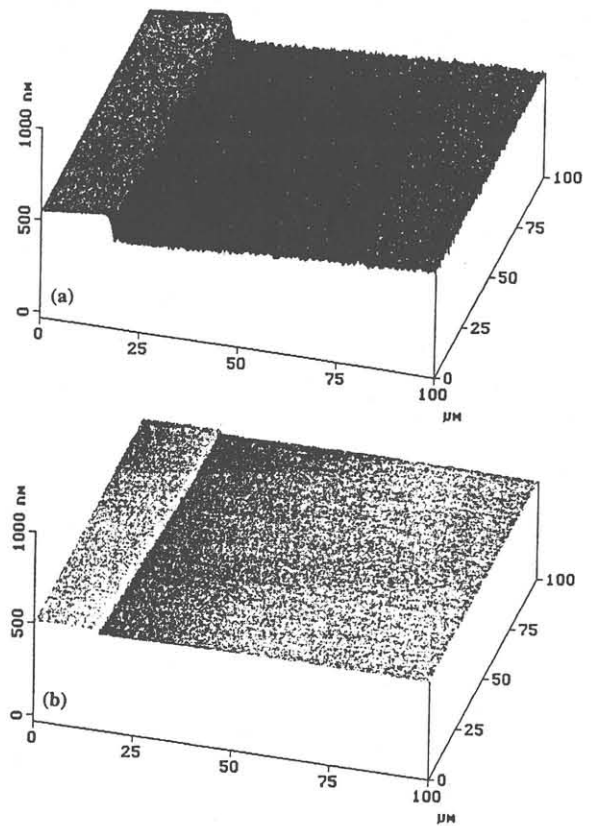

Fig. 4. The AFM micrographs (a) CMP-only process (b) self-align+CMP process.
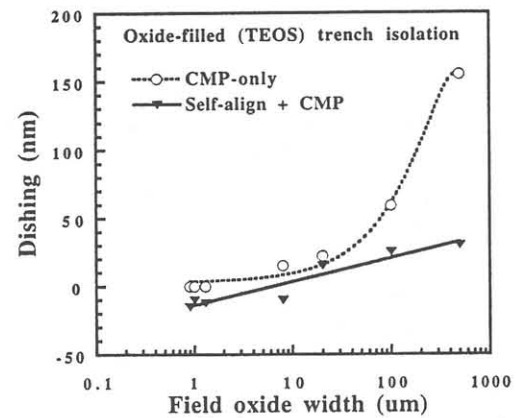(field oxide width = 500 μm)

Fig. 5. The amount of dishing using CMP-only and self-align+CMP processes.
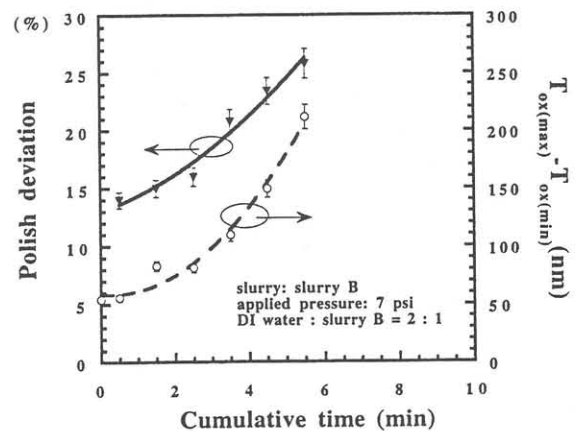

Fig. 6. The deviation during polish and the difference in oxide thickness associated with cumulative polish time.