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Dry O_2 High Pressure Field Oxidation for 0.25 μm Isolation Technology

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Advanced LOCOS isolation using dry O_2 high pressure field oxidation has been investigated for 0.25 μm technology. It is demonstrated that this process satisfies all of the isolation requirements for the 256 Mbit DRAM generation. There is no degradation of the gate oxide. Diode leakages are approximately 6–10 fA/μm and 8 fA/μm^2 at 3.5V. The field threshold and punchthrough voltages are greater than 8 and 10V, respectively. Active devices do not show any significant narrow width effects or abnormal subthreshold characteristics.

1. INTRODUCTION

The lower cost and process simplicity of advanced LOCOS isolation makes it a highly attractive option compared to the other isolation techniques (1-3) that have been proposed for 0.25 μm technology (256 Mbit DRAM). The encroachment with the LOCOS process using atmospheric wet oxidation has limited its application to the 16 Mbit DRAM. LOCOS with wet high pressure oxidation reduces the encroachment and field oxide thinning effect (4), but the encroachment is still too high to be suitable for 0.25 μm applications. This study investigates the use of dry O_2 high pressure field oxidation for advanced DRAM isolation processes.

2. EXPERIMENTAL

Advanced LOCOS isolation using various combinations of pad oxide and pad nitride thickness were used for the fabrication of NMOS active and field devices. Field oxidation was done at 25 atmospheres in a Gasonics high pressure oxidation system at 1000°C and 1100°C in dry O_2 to obtain 250–300 nm oxide. Physical characterization was done using SEM and TEM. The following conditions were used for the electrical characterization: (1) gate oxide: breakdown voltage (BV) at 200 pA/μm^2, (2) diode leakage: current with 3.5V across the junction, (3) field devices: array field subthreshold voltage at 2 fA/cell (Vd = 3.3V, Vb = -1.0V, Vs = 0.0V), threshold voltage at 1 μA/μm (Vd = 3.3V, Vb = -1.0V, Vs = 0.0V), punchthrough voltage at 1 μA/μm (Vg = 0.0V, Vb = -1.0V, Vs = 0.0V),and (4) active devices: extrapolated threshold voltage at Vd = 0.1V, Vb = -1.0V, and Vs = 0.0V.

3. RESULTS AND DISCUSSION

Physical Characterization: Cross sectional profiles for the different combinations of pad oxide and nitride are shown in Fig. 1 for high pressure oxidations at 1000°C and 1100°C. As expected, the encroachment increases with thicker pad oxide and thinner nitrides. However, the temperature does not seem to have a strong effect on the encroachment. Corner encroachment for high pressure dry O_2 and low pressure wet oxidations are shown in Fig. 2. The difference becomes very significant for the dimensions relevant to 0.25 μm technology. The lateral encroachment and the field oxide profiles in the

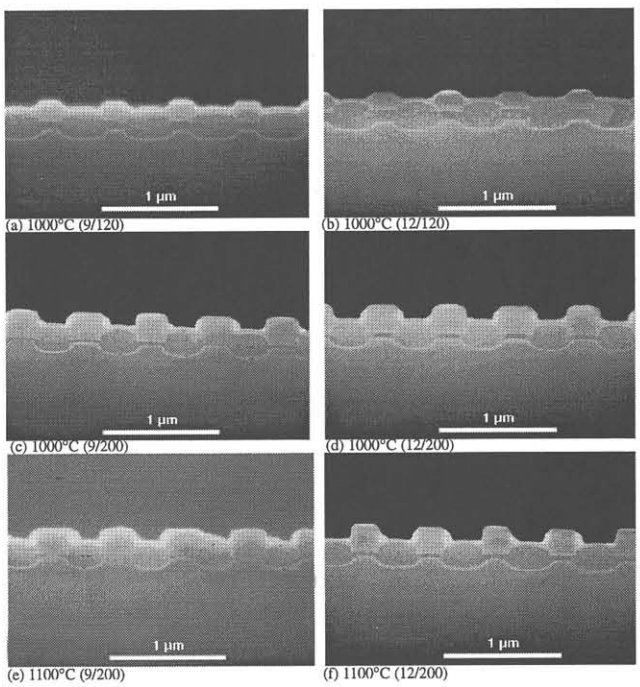

Fig. 1. Cross section profiles (pad oxide/nitride in nm).

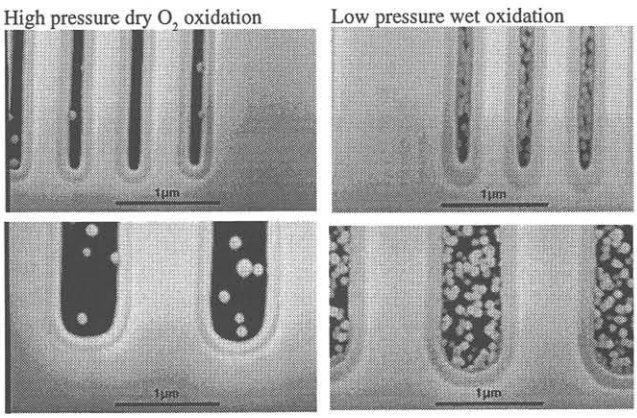

Fig. 2. Corner encroachment.

substrate are shown more clearly in Fig. 3. The high pressure oxidation process results in very low lateral encroachment without any lattice defects. This effect is thought to be due to the change in the viscosity of the oxide at high pressures and/or a difference in the lateral and vertical oxidation rate caused by the stress exerted from the masking stack.

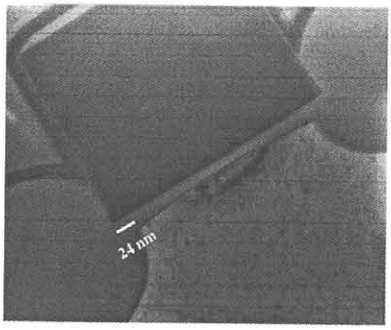

Fig. 3. Lateral encroachment and field oxide profile for dry O_2 high pressure oxidation.

Electrical Characterization: The gate oxide BV for area intensive, gate edge intensive, and array (perimeter intensive) capacitors are shown in Fig 4. When compared to the area intensive structure (intrinsic gate oxide characteristics), the array shows a slightly higher BV. This indicates the possibility of a thicker effective gate oxide in the array due to encroachment/stress. No significant differences were seen for the different pad oxide and nitride combinations or the field oxidation temperature. The current-voltage (I-V) characteristics for the array capacitor are shown in Fig. 5. The results for a test without sacrificial oxidation are also shown in Fig. 5. The kink in the I-V characteristics is under investigation. In this case, it was expected that the dry oxidation process would not generate Kooi defects and hence should eliminate the need for sacrificial oxidation.

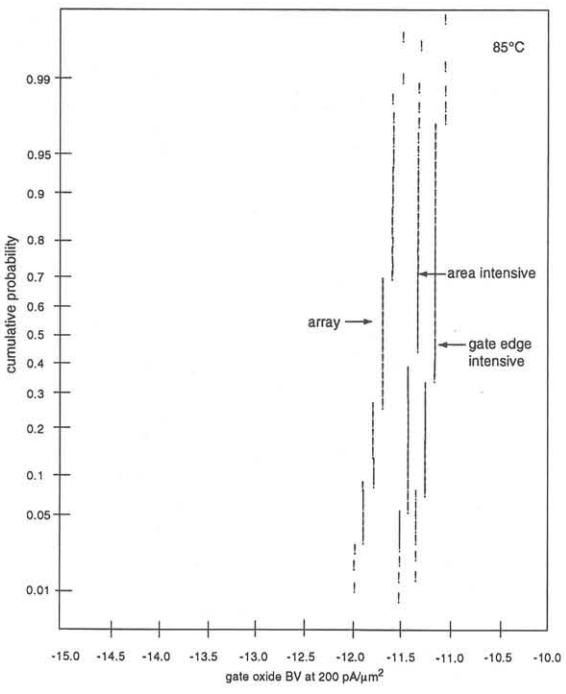

Fig. 4. Gate oxide BV distribution.

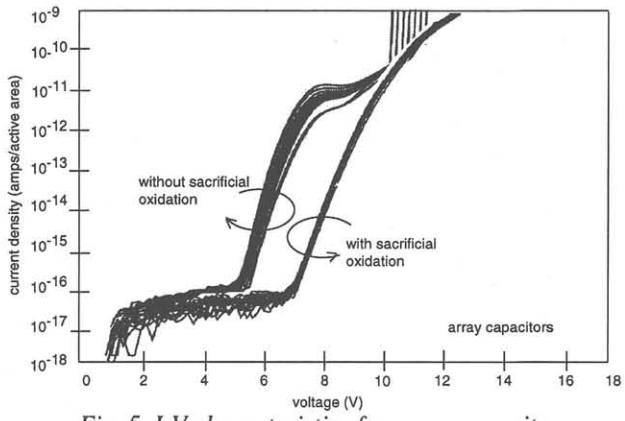

Fig. 5. I-V characteristics for array capacitors.

The diode leakage on area intensive structures was approximately 8 fA/μm2 irrespective of the various process combinations (Fig. 6a). The results for the perimeter intensive structure are shown in Fig. 6b. The leakage is not strongly affected by the pad oxide and nitride combinations used in this test. The optimized oxidation process results in a slightly lower leakage. The 1100°C process shows a larger distribution in the leakage with the high values mainly near the edges of the wafers. The leakage distribution can be further improved by controlling the temperature variation across the wafers.

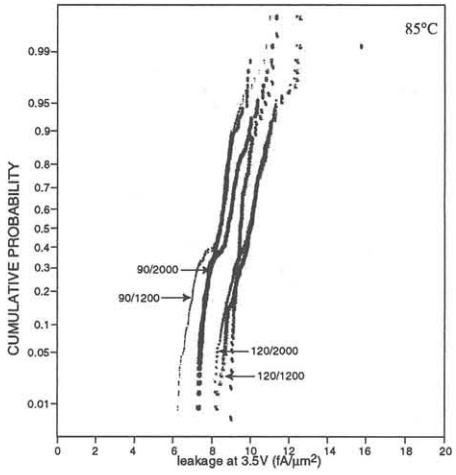

Fig. 6a. Diode leakage on area intensive structures (pad oxide/nitride in Å).

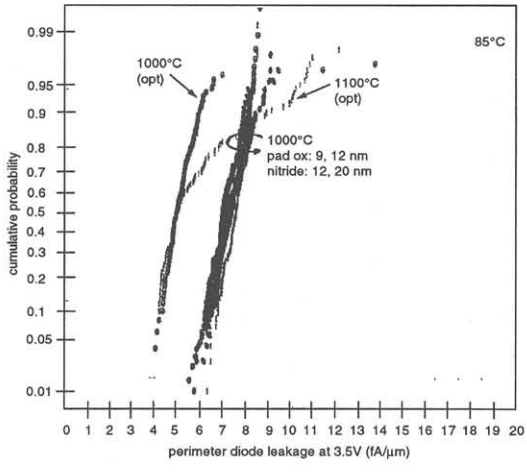

Fig. 6b. Diode leakage on perimeter intensive structures.

The field subthreshold voltage measured on an array structure is shown in Fig. 7. The values are greater than 6.5V for both processes. This value depends on the field oxide thickness in the array and shows a direct correlation with the stack composition, the expected encroachment, and the related field oxide thinning effect. The threshold and punchthrough voltages on isolated field devices are shown in Fig. 8.

The array active devices exhibit good subthreshold characteristics (Fig. 9) and do not show any significant narrow width effects (Fig. 10).

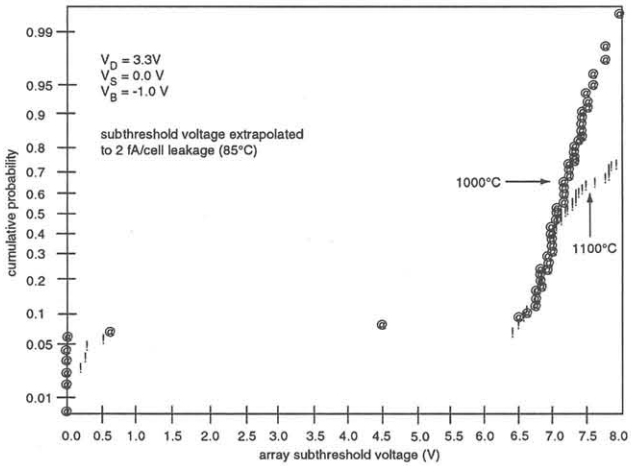

Fig. 7. Array subthreshold voltage distribution.

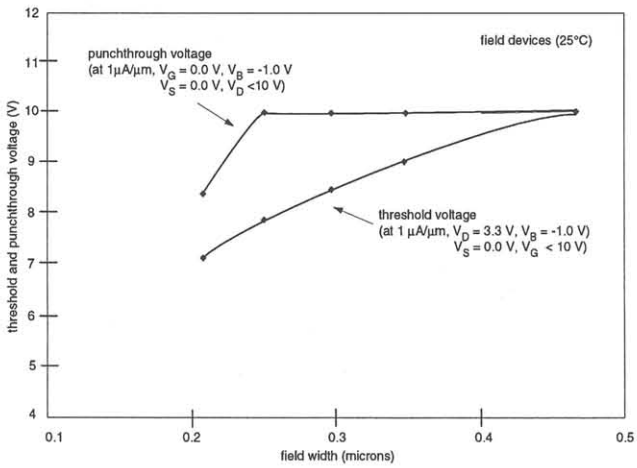

Fig 8. Threshold and punchthrough voltage on isolated field devices.

4. CONCLUSIONS

The feasibility of using a LOCOS process for the 256 Mbit DRAM generation in conjunction with dry O_2 high pressure field oxidation has been demonstrated in this paper. The low stress with this oxidation process should make it possible to extend LOCOS based isolation to the 1 Gbit generation in combination with shallow silicon trench and protective sidewall spacers.

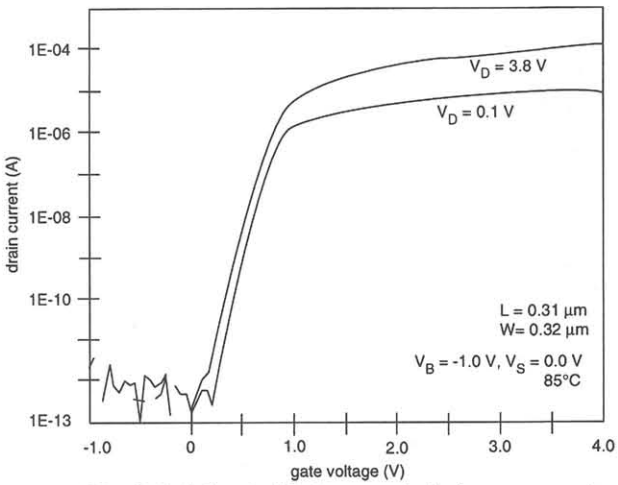

Fig. 9. Subthreshold characteristic for array active device.

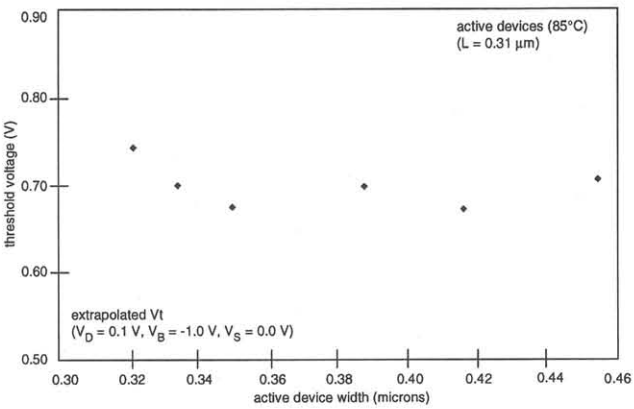

Fig. 10. Threshold voltage for array active devices.

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