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Combination of Chemical Mechanical Polishing and Ultrahigh Vacuum Chemical Vapor Deposition Techniques to Fabricate Polycrystalline Thin Film Transistors

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Top-gate polycrystalline silicon (poly-Si) thin film transistors (TFTs) have been fabricated by ultrahigh vacuum chemical deposition (UHV/CVD) and chemical mechanical polishing (CMP) techniques. UHV/CVD can deposit high quality poly-Si films without long-term recrystallization and CMP can effectively improve the surface morphology. Due to these characteristics, we propose a novel method to fabricate poly-Si TFTs and demonstrate the feasibility of fabricating better performance poly-Si TFTs at low temperature and low thermal budget processes.

1. INTRODUCTION

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) are widely used in integrated circuits[1] and active matrix liquid crystal displays (AMLCDs)[2]. For these applications, poly-Si TFTs provide a much higher carrier mobility than the amorphous silicon (a-Si) ones due to the fine film crystallinity, thus leading to faster switching speed and higher current driving capability. Unfortunately, the high temperature and larger thermal budget processes encounted in conventional growth techniques of poly-Si films restrict the development in these field. Though using laser anneal technique can dramatically enhance the grain growth to obtain high performance TFTs, however, the uniformity and throughput are the problems to overcome. Therefore, it is essential to develop a low temperature or low thermal budget processes without compromising the device performance. In order to meet this requirement, long-term recrystalline treatment is often used, but which may seriously affect the throughput of fabrication. Recently, it was found that high quality poly-Si films can be grown by ultrahigh vacuum chemical vapor deposition system below 550 ℃ [3]. However, the larger surface roughness inheres in these films, which inhibits the top-gate structure from fabricating self-aligned TFTs.

Recent work has shown that the planarized poly-Si surface can improve the field-effect mobility[4]. However, the recrystallization step is still avoidable. In this work we propose and demonstrate a novel approach for fabricating poly-Si TFTs to meet above requirement. This approach utilizes an undoped poly-Si film to form the channel. An UHV/CVD system was employed to prepare the poly film followed by chemical mechanical polishing (CMP). These techniques feature an ultraclean growth environment (base pressure ~ 10^{-9} Torr) as well as the reduced deposition pressures (~ 1 mTorr) and the CMP system to reduce the surface morphology of poly films. Therefore, a higher performance poly-Si TFT is possible to be obtained using UHV/CVD deposited poly-Si films without any post-treatment.

2. EXPERIMENTAL

An 150 nm-thick undoped poly-Si was deposited by UHV/CVD at 550℃ on a 150-mm silicon wafer with a 300 nm-thick thermal grown oxide and the uniformity is within 10 %. The undoped poly-Si film was employed as the channel layer and its grain size was around 80 nm, as measured by plane view transmission electron microscopy (TEM). The channel layer was polished to about 77 nm by CMP and the uniformity was still preserved then defined by a photomask and patterned by plasma etching for the active area island. A 30 nm-thick gate oxide was then thermally grown at 900 ℃ in dry Oxygen ambient. After these steps, a 300 nm-thick poly-Si was deposited by low pressure chemical vapor deposition (LPCVD) at 620 ℃ as the gate material and source/ drain doping mask, which was also defined by a photomask patterning. The gate electrode and source/ drain regions were doped by $POCl_3$ at 850℃ for n-channel and doped by BN source at 900℃ for p-channel, respectively. A 400 nm-thick passivation oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD). After the passivation layer deposition, contact holes were defined and a 500 nm-thick aluminum film metalization was performed followed by a 400 ℃ anneal in nitrogen ambient for 30 min.

3. RESULTS AND DISCUSSION

The roughness of the poly-Si film was observed by atomic force microscopy (AFM) which were shown in Fig. 1(a) and Fig. 1(b) for unpolished and polished ones, respectively. The scanned area is 5 μm X 5 μm. The average surface roughness of the poly-Si film had been dramatically reduced from 9.0 nm to 3.7 nm after polishing, which indicates CMP can polish poly film effectively. Typical transfer curves for p- and n- channels are shiwn in Fig. 2 and Fig. 3, respectively. Fig. 4 and Fig. 5 illustrate the density of states in band gap and the activation energy, respectively. The density of states were obtained by field-effect conductance method[5,6]. The lower density of states and steeper activation energy curves can explain the lower threshold voltage and subthreshold slope characteristics are better than which grown by conventional LPCVD. On the other hand, by Fig. 5 we can estimate the band gap[7] is about 0.983 eV. The fermi level locates slightly below the

midgap (below 0.063) which indicates the poly film is slightly p type, and the hump (dangling bonds) also near but slightly below midgap. These results are consists with which deposited by LPCVD. In Fig. 5, the kink also exists in the activation curve of p-channel TFTs, which may be due to the dangling bond in midgap but the real mechanism is under study. The device has a channel length of 20 μm and a width of 100 μm, and $I_{ON}/I_{OFF} \approx 2 \times 10^6$ for both p- and n-channels. The subthreshold slopes are around 0.4 V/decade and threshold voltages are around 5 V. The better characteristics is mainly attributed to the high quality poly film deposited at ultraclean environment and partial due to reduced surface roughness. Because in such a low pressure, the oxygen and carbon concentrations are below the secondary ion mass spectroscopy (SIMS) detection limit, which results in low trap density in poly films. Another reason is due to the reduced surface roughness but the roughness is still larger than LPCVD-grown films (~1 nm) and the high temperature oxidation process will alter the surface roughness of poly films, which also enhance the leakage current. Detailed device characteristics are summarized in Table 1. All parameters were measured at drain voltage, V_d= 0.1 V except for I_{ON}/I_{OFF} was measured at V_d= 5 V. We must emphasize that the performance was obtained without any post-treatment. How to furtherly improve the surface morphology, deposit gate oxide at low temperature, and to passive devices by plasma treatment to obtain high performance devices is underway.

4. CONCLUSIONS

In conclusion, we have developed a novel process for fabricating poly-Si TFTs using CMP and UHV/CVD techniques, which demonstrated the feasibility of fabricating poly-Si TFTs at low temperature and low thermal budget although present gate oxide and source/ drain doping are still using high temperature processes. Our work reveals that the usage of these techniques for device fabrication would be a potential approach to obtain better performance, high throughput process steps.

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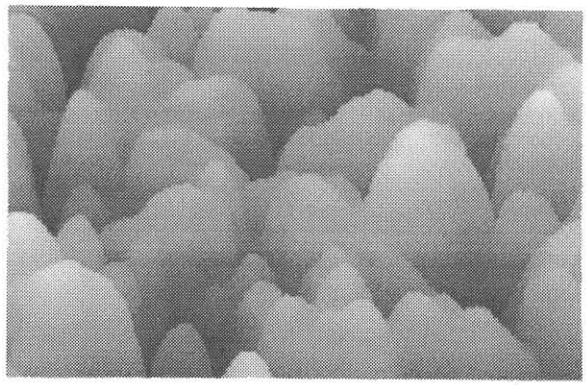

Fig. 1(a) The unpolished poly-Si film which average surface roughness is about 9.0 nm observed by AFM.

Fig. 1(b) The polished poly-Si film which average surface roughness is about 3.7 nm observed by AFM.

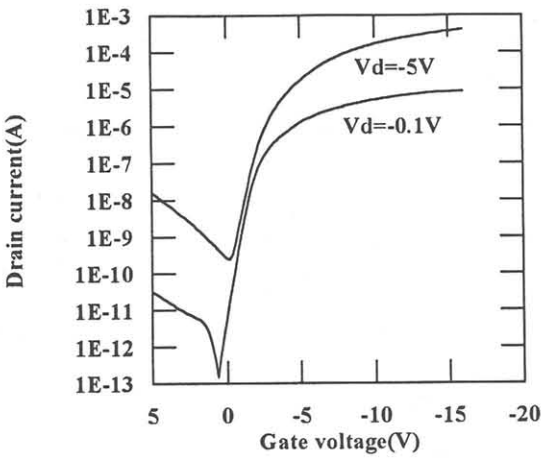

Fig.2 Drain current versus gate voltage of p-channel TFT

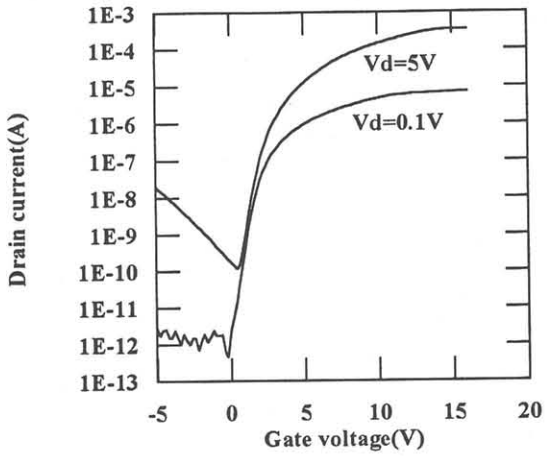

Fig.3 Drain current versus gate voltage of n-channel TFT

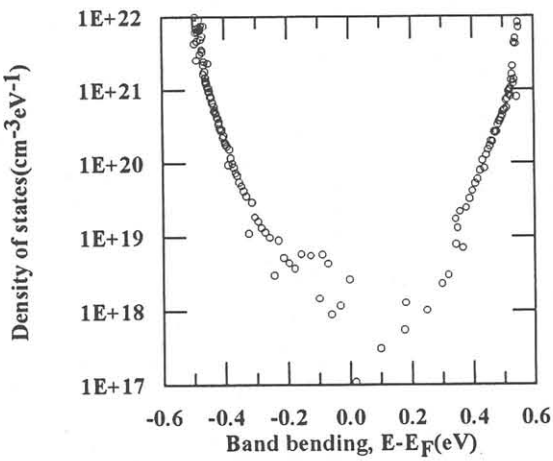

Fig.4 Density of states in band gap

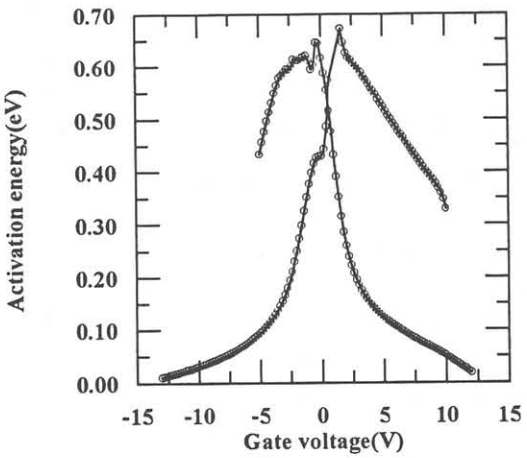

Fig.5 Activation energy versus gate voltage

Table 1 The detailed characteristics of devices

samples & parameters	field effect mobility (cm^2/V-s)	threshold voltage (V)	subthreshold slope (V/decade)	trap states (cm^{-2})	I_{ON}/I_{OFF}
p-channel	14.3	-5.4	0.45	$4.0X10^{12}$	$2X10^6$
n-channel	16.6	4.2	0.42	$3.5X10^{12}$	$2X10^6$