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Preamorphization of the Channel Region of MOS Devices for Shallow Counter Doping

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Channel preamorphization, which is a technique used for shallow boron counter doping in pMOSFETs to suppress short-channel effects, improves gate oxide quality in MOS capacitors with the field-edge structure. This would be due to the gettering effect of small dislocation loops induced near the original amorphous/crystalline interface. The leakage current of junction diodes is increased by channel preamorphization. This will be improved by increasing the preamorphization depth.

1. Introduction

For buried-channel pMOSFETs, a shallow boron counter-doped layer in the channel region is effective in suppressing short-channel effects.[1] We have devised a novel technique for shallow boron counter doping that includes channel preamorphization (CP) by Si ion implantation, and have reported excellent effects on shallow boron-doped layer formation and short-channel-effect suppression in pMOSFETs.[2,3] This paper shows how channel preamorphization affects the quality of gate oxides as thin as 50 Å and S/D leakage characteristics.

2. Device fabrication

CZ, n-type (100) Si wafers were used. Active regions were delineated by the LOCOS process. Prior to channel ion implantation, Si ions were implanted at 180 keV and a 2×10^{15}-cm^{-2} dose through a 150-Å temporary oxide to amorphize the surface. This was followed by the channel ion implantation of BF_2, arsenic and phosphorus. After etching off the temporary oxide, a 50-Å gate oxide was grown in dry O_2 ambient at 800 ℃. Phosphorus-doped polysilicon was then deposited as the gate material, and the gate pattern was defined and etched. S/D junctions as shallow as 800 Å were formed. Relatively deep (2000 Å) p^+ layers were formed in the S/D contact regions prior to metallization to prevent Al spiking.

3. Results and discussion

(A) Gate oxide quality estimated from measurement of MOS capacitors

Figure 1 shows yields of MOS capacitors at the gate voltage of 6 V (about 12 MV/cm). Type (a) was a 200 x 200 μm^2 capacitor without field oxide edge under the gate electrode (gate-edge structure). Type (b) was a 200 x 200 μm^2 capacitor with field oxide edge under the gate electrode (field-edge structure). Type (c) also had the field-edge structure with the same area as (b), but its periphery was 50 times larger. For MOS capacitors with the gate-edge structure, yield is good irrespective of whether the channel was preamorphized or not. For MOS capacitors with the field-edge structure, yield is good for capacitors with CP, while yield is reduced without it, and the difference in the yield due to CP is enhanced for the capacitors with larger peripheries. Figure 2 and 3 respectively show results of TDDB measurements of MOS capacitors with the field-edge structure and the gate-edge structure. It can be seen that CP improves the TDDB characteristics of MOS capacitors with the field-edge structure, while those of MOS capacitors with the gate-edge structure are good for both capacitors. These results coincide with the result shown in Fig. 1, indicating that the source of gate oxide quality degradation is located near the field oxide edge and is eliminated by channel preamorphization process. It is thought that the small dislocation loops near the original amorphous/crystalline interface induced by preamorphization[2,4,5] act as gettering sites for contaminants that would be around the field oxide edge, which results in the improved gate oxide quality.

(B) Leakage characteristics of junction diodes

Leakage characteristics of 100 x 100 μm^2 junction diodes are shown in Fig. 4. In these diodes, there are 25 0.4 x 0.4 μm^2 contact holes, and the junction depth of the contact regions is about 0.2 μm, while the junction

depth of other regions is as shallow as 800 Å. The leakage current with CP is larger than without it. The degradation is greater for higher voltage. Figure 5 compares leakage characteristics between two types of junction diodes with CP. Curve (a) is for the diodes shown in Fig. 4 (diode (a)), and curve (b) for diodes with 4851 contact holes (diode (b)). The contact regions of diode (b), which are 0.2 μm deep, are 194 times larger than (a). For voltages lower than 1 V, leakage current for diode (b) is about two orders of magnitude larger than diode (a). This ratio is close to the ratio of the contact region area. This means that leakage current for voltages lower than 1 V mainly arises from contact regions, or deep regions, and that the leakage current of shallow regions is small. This can be understood by considering that defects located near the original amorphous/crystalline interface[4,5] are in the depletion layer of the contact regions, and not in the depletion layer of the shallow regions. This is schematically illustrated in Fig. 6 by curve (a), which shows the depletion layer edge. As applied voltage is increased, the ratio of leakage current gradually decreases and becomes 1 at about 2.5 V. This can be understood by considering that the depletion layer extends to contain more defects as applied voltage is increased, and eventually, all defects come to be located in the depletion layer. This is schematically illustrated in Fig. 6 by curve (b). There were no differences in the leakage characteristics of junction diodes without CP between diode (a) and diode (b), since the defects arising from CP were not present. From these results, it is expected that the leakage current of junction diodes with CP will be decreased by increasing the preamorphization depth or reducing the junction depth of S/D.

4. Summary

The influences of channel preamorphization on the quality of gate oxides and S/D leakage characteristics have been studied. Channel preamorphization improves gate oxide quality in MOS capacitors with the field-edge structure. This would be due to the gettering effect of small dislocation loops induced near the original amorphous/crystalline interface. The leakage current of junction diodes is increased by channel preamorphization. This will be improved by increasing the preamorphization depth.

References

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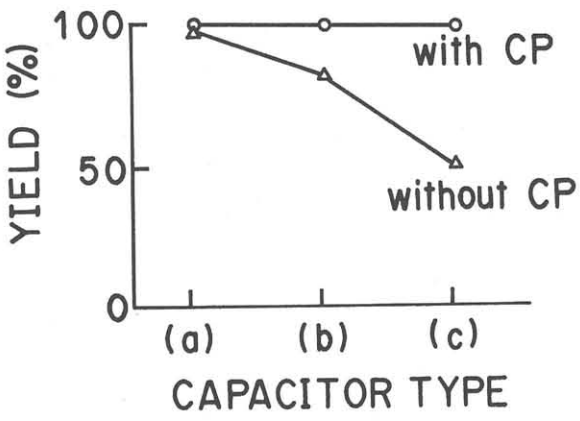

Fig. 1 Yields of MOS capacitors with channel preamorphization (CP) and without it. Gate voltage is 6 V.

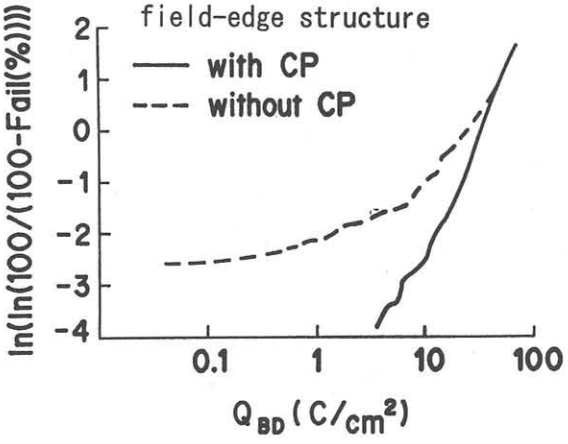

Fig. 2 Weibull plots of TDDB data for MOS capacitors with the field-edge structure.

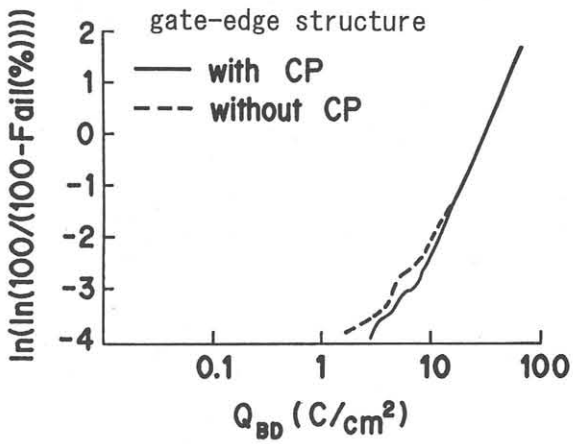

Fig. 3 Weibull plots of TDDB data for MOS capacitors with the gate-edge structure.

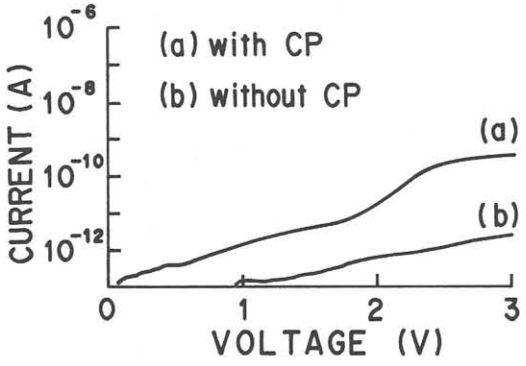

Fig. 4 Leakage characteristics of junction diodes (a) with CP and (b) without it.

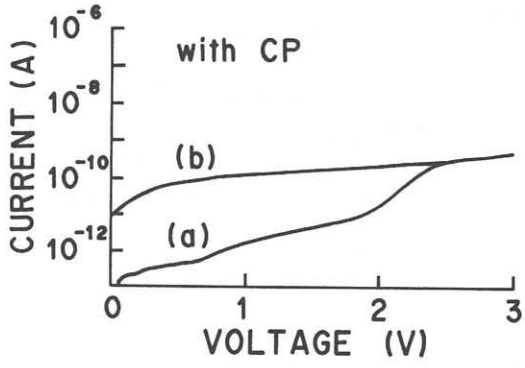

Fig. 5 Comparison of leakage characteristics between two types of junction diodes with CP.

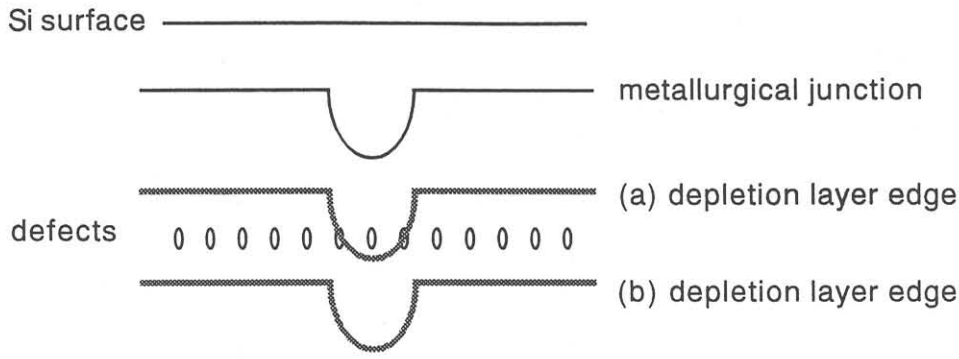

Fig. 6 Schematic of junction diodes with CP showing the depletion layer edges at (a) low voltage and (b) high voltage.