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Identification of MOS Gate Dielectric-Breakdown Spot Using High-Selectivity Etching

Rinji SUGINO, Toshiro NAKANISHI, Kanetake TAKASAKI, and Takashi ITO

Fujitsu Laboratories Ltd.
10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

We have developed a simple method of identifying dielectric-breakdown spots in gate oxides by using high-selectivity Cl-radical etching. This method is based on the phenomenon where Cl radicals selectively etch the crystallized Si corresponding to the breakdown spot in the gate oxide. The crystallized Si in the gate oxide was produced by intrinsic breakdown. Applying this method to a MOS diode with a 6 nm gate oxide, we observed one breakdown spot from a gate oxide area far from the LOCOS edge.

1. Introduction

As gate oxides become thinner, the analysis of dielectric-breakdown becomes more important for improving manufacturing processes of advanced MOS ULSI devices. It is well known that a breakdown spot in the gate oxide depends on the conditions of some processes, such as isolation[1, 2], sacrificial oxidation, and electrode deposition. Optical methods, such as the optical beam induced current system[3] and the emission microscope method,[4] have usually been used to identify the breakdown spot. These optical methods are sensitive to weak points in the gate oxide but need empirical knowledge to distinguish between a leakage current and dielectric-breakdown. The phosphorous thermal-diffusion method[5] and the liquid crystal method[6] are also known as applied process methods. These are used even now as a relatively easy method but they show a poor ability to precisely identify the breakdown spot.[7] On the other hand, the application of an etching technique is expected to be both simple and sufficiently precise to identify the breakdown spot.

We have studied a Si etching technique using Cl radicals generated by UV irradiation with high-selectivity for an SiO_2 layer.[8] Cl radicals never react with Si-O bonds, and hardly penetrate SiO_2 network structures. These characteristics explain why Cl radicals etch a Si substrate through a native oxide layer on the surface. We attempted to identify the breakdown spot using this high-selectivity etching technique.

In this paper, we describe the principle and method of identifying the breakdown spot using high-selectivity Cl-radical etching. Of particular interest is the relationship between the appearance of the breakdown spot with this etching method and the electric stress applied to the gate oxide. In addition, we discuss the local destruction of the gate oxide due to dielectric-breakdown based on transmission electron microscopy (TEM) observation.

2. Experiment

The process to identify a breakdown spot is shown in Figure 1. The sample used was a MOS diode fitted with a 6 nm gate oxide on a *p-type* Si substrate, 150 nm poly-Si gate, and a 0.04 mm^2 gate area, which reached dielectric-breakdown. Cl-radical etching was carried out straight after poly-Si etching under the following conditions: High-purity Cl_2 gas maintained at 2.7 kPa during etching, a temperature of 420°C, and UV of 200-300 nm wavelength at 22 mW/cm^2 irradiated for 15 minutes. When using these conditions for Si (100) without native oxide, the etched depth corresponded to 5 μm.

During over-etching, a cave-like etched region in the Si substrate was produced under the breakdown spot of the gate oxide. Although Cl radicals do not penetrate SiO_2 at all, they can etch the Si substrate through the breakdown spot which acts as the etching-path. The breakdown spot could be found easily by focusing the optics on the gate oxide located at the center on the etched region of Si substrate.

3. Results and Discussion

3-1 Breakdown spot observation

From optical microscopy observation, as shown at the top of Figure 2, the etched region was observed through 6 nm gate oxide which also remained after etching. By scanning electron microscopy (SEM), focusing on the center of the etched region, a breakdown spot with a size of about 0.1 μm was observed as a defect in the gate oxide, as shown at the bottom of Figure 2. As can be seen from surface images, breakdown occurred at the 6 nm gate oxide area far from the LOCOS edge. In addition, only one etched region with a breakdown spot was observed for each MOS diode reaching dielectric-breakdown. This means dielectric-breakdown finally occurred at one point in the gate oxide.

3-2 Dependence of leakage current

To investigate the relationship between the appearance of the breakdown spot using this etching method and the electric stress in the gate oxide, we carried out Cl-radical etching for the MOS diode after applying several voltages. Figure 3 shows the mapping of the leakage currents for voltages between -6.0 V to -9.6 V applied to the MOS diodes. The shaded chips in Figure 3 are diodes which have breakdown spots found by Cl-radical etching method. When higher electric fields were applied to diodes and after undergoing a leakage current in the order of 10^{-3} A, we could recognized the breakdown spot.

These diodes, having undergone a leakage current in the order of 10^{-3} A, show intrinsic dielectric-breakdown. As shown in the C-V characteristics in Figure 4, the diode having intentionally undergone this leakage current indicated an initial short-circuit. On the other hand, the diode having intentionally undergone a leakage current in the order of 10^{-4} A did not reach intrinsic breakdown, although the leakage current at the applied voltages between -3 V and -5 V was slightly higher than the reference one. These results suggest that the appearance of a breakdown spot by high-selectivity Cl-radical etching corresponds to the intrinsic dielectric-breakdown of the MOS diode, and that the current leakage path in the gate oxide generated by this intrinsic breakdown is consistent with the etching-path for penetrating Cl radicals.

3-3 Gate oxide structure after breakdown

The structure of the MOS diode after intrinsic breakdown was observed by transmission electron microscopy (TEM). Figure 5 shows the dark field image of the MOS diode after reaching intrinsic breakdown at -9 V. The TEM sample was prepared by thinning with a focused ion beam after marking the breakdown spot identified by emission microscopy. As shown in this image, part of the gate oxide has become white, and region in the Si substrate includes defects and dislocations. The white part in the gate oxide suggests crystallization, possibly Si crystallized, because the SiO_2 crystal would be decayed by electron irradiation during TEM observation.[9] The local SiO_2 structure in the gate oxide layer may be converted to crystallized Si by "thermal-breakdown"[5] due to the electric stress related to intrinsic breakdown. The locally crystallized Si in the gate oxide acts as the current leakage path, resulting in the diode short-circuit. These results support one model of breakdown suggested by Hasegawa et al.[10] where dielectric breakdown seems to occur after a sufficient number of Si-Si bonds have formed.

Consequently, Cl radicals can etch a Si substrate under the breakdown spot, and then etch the breakdown spot i.e. part of the crystallized Si in the gate oxide produced by intrinsic dielectric-breakdown. On the other hand, the breakdown spot hardly appeared in the MOS diode which did not reach the intrinsic dielectric-breakdown by this high-selectivity Cl-radical etching method.

4. Conclusion

We have successfully identified an intrinsic dielectric-breakdown spot by Cl-radical etching. Using this method for a MOS diode with a 6 nm gate oxide, only one breakdown spot was observed from a gate oxide area far from the LOCOS edge. Cl radicals etch the breakdown spot where part of the crystallized Si in the gate oxide is produced by intrinsic dielectric-breakdown. The local SiO_2 structure in the gate oxide layer was converted to crystallized Si due to the electric stress related to intrinsic breakdown. The locally crystallized Si in the gate oxide acts as the etching-path for the Cl radicals.

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References

1) J. Yugami and A. Hirasawa, *in Proc. ICMTS*, vol. 4, (1991) p17.
2) H. Uchida, N. Hirashita, and T. Ajioka, IEEE Trans. Electron Devices, **40** (1993) 1818.
3) K. Haraguchi, *in Proc. Electron Beam Testing Symp. 121th Meeting* (Osaka, JAPAN) p140, Dec. 1992
4) N. Khurana and C. L. Chiang, in Proc. *in Proc. IEEE Int. Rel. Phys. Symp.*, (1987) p72.
5) K. Yamabe, K. Taniguchi, and Y. Matsushita, in Proc. *in Proc. IEEE Int. Rel. Phys. Symp.*, (1983) p184.
6) J. M. Soden and C. F. Hawkins, *IEEE Des. Test*, Aug. (1986) p56.
7) T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, IEEE Trans. Electron Devices, **39** (1992) 537.
8) R. Sugino, Y. Nara, H. Horie, and T. Ito, J. Appl. Phys., **76** (1994) 5498.
9) N. Suyama, private communication.
10) E. Hasegawa, K. Akimoto, M. Tsukiji, T. Kubota, and A. Ishitani, *in Ext. Abst. of the 1993 Int. Conf. of SSDM.*, (1993) p86.

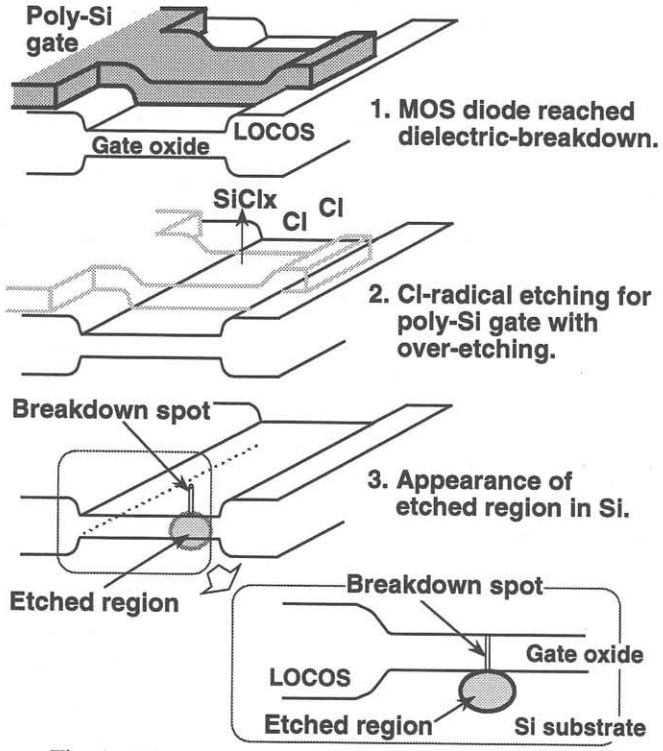

Fig. 1. The process to identify the breakdown spot of a MOS diode by high-selectivity Cl-radical etching.

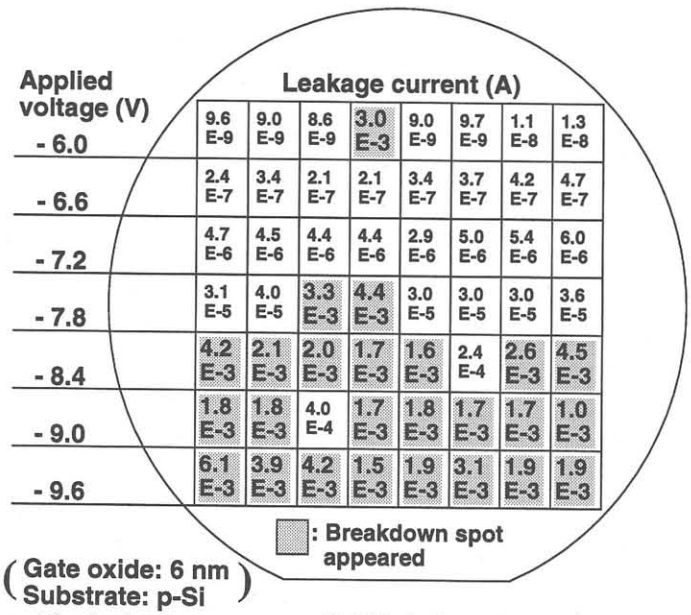

Fig. 3. Leakage currents of MOS diodes under several applied voltages. And the shaded chips are diodes which have breakdown spots found by Cl-radical etching.

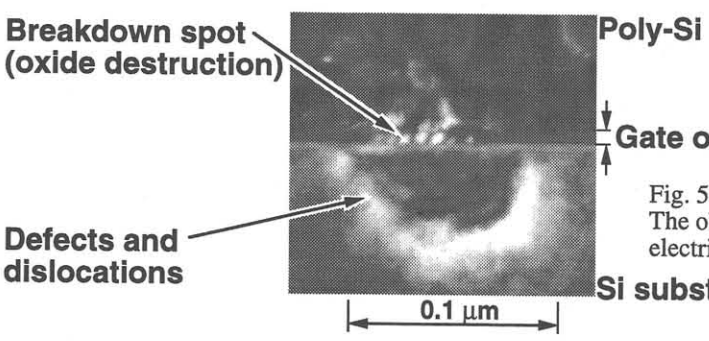

Fig. 5. Dark field image of cross-sectional TEM. The observed sample was MOS diode with appeared electric stress of -9 V.

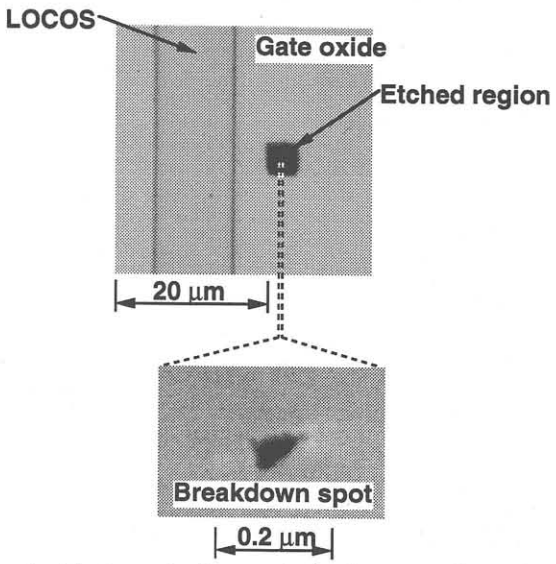

Fig. 2. Photographs from optical microscopy image (top) and SEM image (bottom) after Cl-radical etching of MOS diode with 6 nm gate oxide.

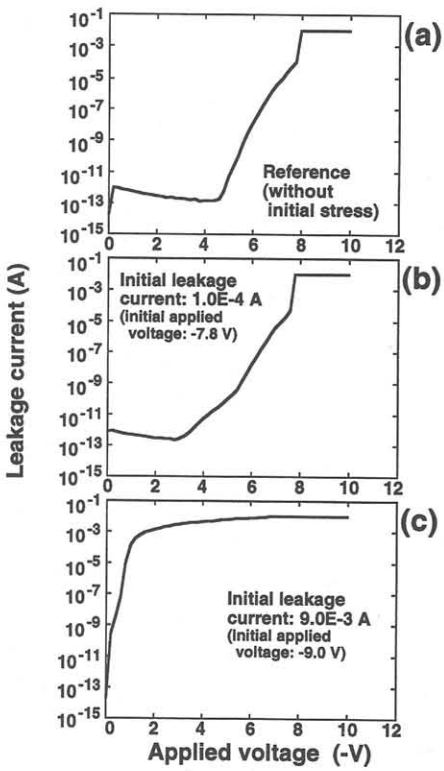

Fig. 4. I-V characteristics of MOS diodes. The initial stress was applied prior to I-V measurement. (a) Reference sample without stress, (b) not reaching dielectric-breakdown, and (c) resultant initial-short by intrinsic breakdown.