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Electrical Characterizations of Pt/(Ba,Sr)TiO_3/Pt Planar Capacitors for ULSI DRAM Applications.

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ABSTRACT : Pt/(Ba,Sr)TiO_3/Pt capacitors are fabricated using DC and RF sputtering process on thermally oxidized silicon wafers for ULSI-DRAM applications. BST thin film deposited at 640℃ with 20nm thickness shows equivalent SiO_2 thickness of 0.35nm and leakage current density, measured at the applied bias of 1.5V and temperature of 83℃, less than 200nA/cm^2. The post-annealing at 750℃ after the top electrode fabrication is very important to obtain a low leakage current level.

1. Introduction

(Ba,Sr)TiO_3 (BST) thin films attract great interest as a new dielectric material of capacitors for the next generation of ULSI-DRAMs due to its high dielectric constant and low leakage current compared to $SrTiO_3$ and Pb(Ti,Zr)O_3 (PZT). Platinum is being widely accepted as the top and bottom electrode material because of its excellent oxidation resistance and chemical stability. However, the electrical properties, such as dielectric constant and leakage current of Pt/BST/Pt capacitor, are very dependant on the fabrication process of the electrodes and the post-deposition treatments as well as the BST film deposition conditions. In this paper, the capacitance and leakage current characteristics of the Pt/BST/Pt capacitors fabricated by sputtering processes are presented, especially in the BST films with thicknesses ranging from 50nm to 15nm. The post annealing effect on the leakage current of the capacitor is also studied for the process integration.

2. Experimentals

Planar Pt/BST/Pt capacitors are fabricated by the sequential deposition of DC sputtered Pt, RF sputtered BST and DC sputtered Pt thin films on thermally oxidized 6″, (100) Si wafers. The bottom Pt electrodes are deposited at 400℃ to obtain hillock free films and a low DC power is used to minimize the surface damage of the BST films during the top electrode deposition. BST thin films are deposited at temperatures ranging from 600℃ to 680℃ in a sputtering gas pressure of 10mTorr. Sputtering gas is 80% Ar and 20% O_2 and a 4″ size sintered target of [Ba]/[Sr] of 50/50 is used. Capacitor areas of $1x10^{-4}$, $3x10^{-3}$ and $1x10^{-2}cm^2$ are defined by dry etching of the top electrodes using an Ar/Cl_2 etching gas and a photo resist mask. The capacitors are annealed at 550℃, 650℃, 750℃ and 850℃ after the top electrode etching. Capacitance and leakage current density of the capacitor are measured using a HP-4284 LCR meter and a HP-4145B semiconductor parameter analyzer.

3. Results

Figure 1 shows the variation of dielectric constants and SiO_2 equivalent thickness (t_{oxeq}) of 50 nm thick BST films as a function of deposition temperatures. RBS analysis showed that the ([Ba]+[Sr])/[Ti] ratio of the films turns out to be about 0.98 ± 0.01 nearly irrespective of the deposition temperatures. XRD analysis showed an improved crystallinity when the deposition temperatures increased, which results

in the increased dielectric constants.

Figure 2 shows the variations of t_{oxeq} and leakage current density, measured at a bias voltage of 1.5V, of the BST films deposited at 640℃ and 660℃ as a function of their physical thicknesses. The t_{oxeq} of the BST film does not decrease linearly with the film thickness because the dielectric constant also decreases with the film thickness. The minimum of t_{oxeq} of 0.35nm is achieved when the film is deposited at 640℃ with its thickness of 20 nm. The leakage current increases slowly until the film thickness decreases down to the critical thicknesses, which is about 20 nm. The leakage current increases abruptly as the film thicknesses decreases to a value lower than the critical value.

Figure 3 shows the leakage current variation of a 20 nm thick BST film deposited at 640℃ measured at room temperature and 83℃ when a positive bias is applied to the top electrode. The leakage current level at 83℃ is marginally acceptable for the 1G DRAM applications.

The leakage current density is critically dependant on the post-annealing temperature after the top electrode deposition. Fig. 4 shows the leakage current density variation as a function of applied bias voltage of a 50 nm thick BST thin film, which is deposited at 660℃ and post-annealed at 550℃, 650℃, 750℃ and 850℃, respectively, for 30 min. when the negative bias voltage is applied to the top electrode. The sample annealed at 750℃ shows the minimum leakage current density. The major charge carriers are the injected electrons from the top electrode when the negative bias is applied to the top electrode and their transport is limited by the potential barrier at the Pt/BST interface - Schottky barrier - due to the difference between the work function of Pt and electron affinity of the BST (1). However, the potential barrier formed at the interface between the top Pt electrode and BST is not as high as that at the interface between the bottom Pt electrode and BST because of the difference in the thermal history of which the two interfaces experienced. High temperature annealing, up to 750℃, improves the top interface quality and greatly reduces the negative leakage current density as shown in Fig. 4. However, the annealing at 850℃ increases the leakage current again by a small amount probably due to the grain growth of the Pt and BST films, as shown in Fig. 4, which in turn increases the interface roughness. Figure 5 shows the surface morphologies of the 50 nm thick BST thin films deposited at 660℃ and post-annealed at (a) 550℃, (b) 650℃, (c) 750℃ and (d) 850℃ for 30 min., respectively. The grain size of the BST film does not change after the annealing at temperatures up to 750℃, but the sample annealed at 850℃ shows larger grains and increased surface roughness.

4. Conclusions

Sputter deposited Pt/BST/Pt capacitor shows good electrical properties for the ULSI-DRAM applications. The minimum t_{oxeq} is about 0.35 nm and its leakage current density is less than 200 nA/cm^2 at $\pm$1.5V and 83℃ when the BST film is deposited at 640℃ with a thickness of 20 nm. The BST films deposited at temperatures higher than 680℃ showed electrically leaky characteristics. The leakage current levels are critically dependant on the post-deposition annealing temperature after the top electrode fabrication. Post-annealing at 750℃ is the best condition to suppress the leakage currents.

5. References

(1) C.S.Hwang, H.J.Cho, S.O.Park, C.S.Kang, H.K.Kang and S.T.Ahn, "Electrical characterization of very thin $SrTiO_3$ thin films deposited by RF sputtering method", submitted to Jpn. J. of Appl. Phys.

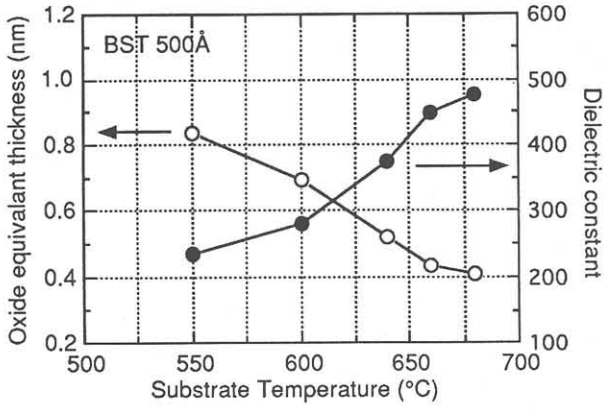


Figure 1. The variation of dielectric constants and Toxeq as a function of deposition temperature.

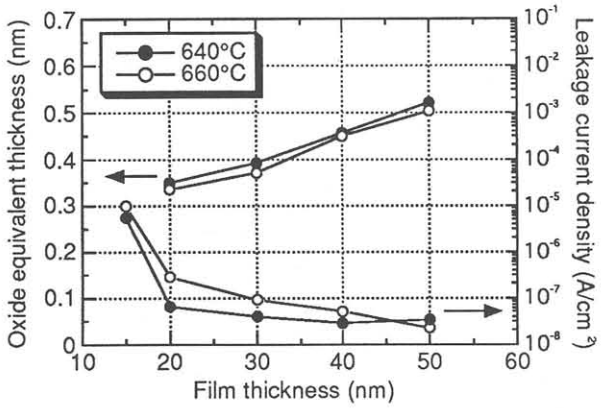
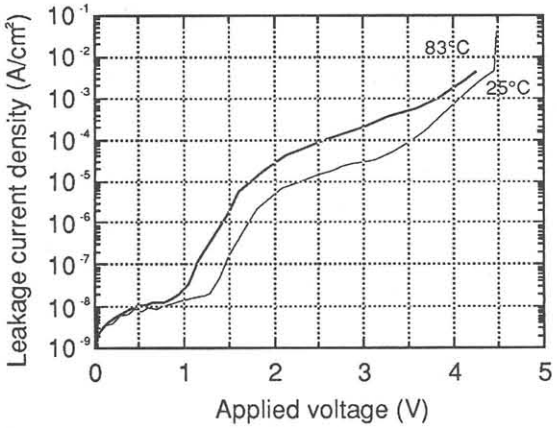


Figure 2. The variation of Toxeq and leakage current density as a function of physical thicknesses.



Fiiure 3. The leakage current variation of a 20nm thick BST film deposited at 640°C.

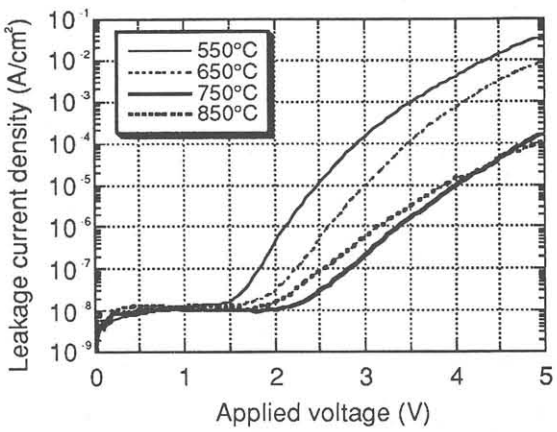


Figure 4. The leakage current density with regard to anneal temperature after top electrode deposition.

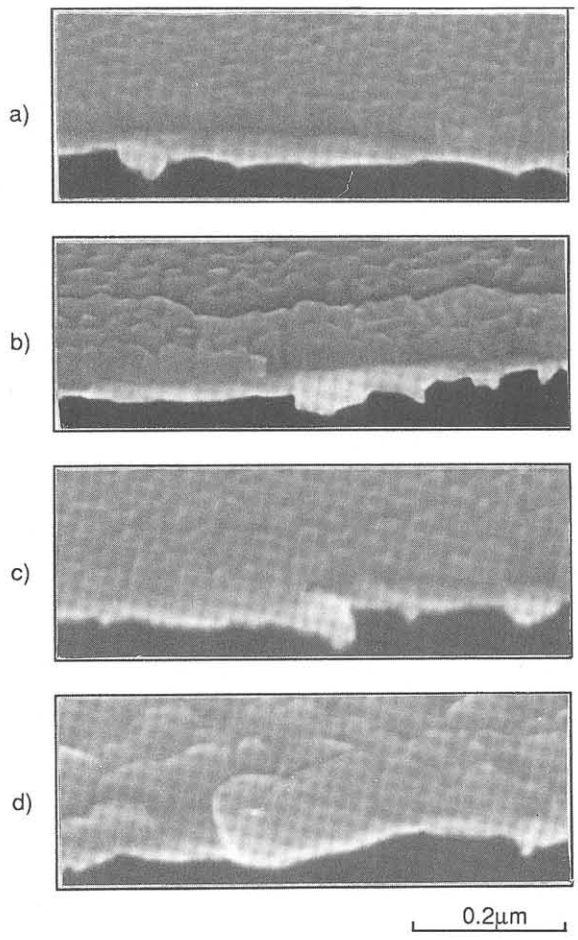


Figure 5. The surface morphologies of the 50nm BST film annealed at a) 550°C, b) 650°C, c) 750°C, d) 850°C