All-Perovskite Ferroelectric/Semiconductor Field Effect Transistor

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Properties of a prototype ferroelectric FET, which was previously proposed by us for a non-volatile memory, are reported. The device used typically a 200µm long and 50µm wide gate and a heavily hole(p)-type-doped channel. The most of the device retained about 50% of initial modulation for 2 weeks, and some retained for 10 months, which markedly surpasses the previous reports on the memory retention. The proposed device should not only improve some performances of ferroelectric FETs but also simplify the memory cell structure and the fabrication processes.

1. BACKGROUNDS

Non-volatile memories for portable apparatus have been regarded as a promising application of solid state devices. However, growing demands for high capacity memories have promoted innovations in the disk memories and the markedly rapid increase of the memory density. A 2.5inch ϕ rigid disk would attain the capacity of 1000Gb in the near future without increasing the production cost. Although this density is theoretically feasible for the conventional Si devices, their production cost and increasing complexity would render them impractical and incompetitive.

Recently, novel approaches to the non-volatile solid state memory are actively investigated, which include the single electron transistor memories and the ferroelectric memories. As for the latter, DRAM(capacitor)-type ferroelectric memories (FRAM) are mainly studied at present. However, the reasonably high memory density, which makes the solid state memory unobsolete in comparison with disk memories, can only be achieved by the FET-type ferroelectric memories.

FET-type ferroelectric memory, i.e., ferroelectric FET (f-FET), which uses ferroelectric as a gate insulator, has been studied for a long time since 1957¹. Almost all types of approaches to overcome these difficulties, which are currently perused, were already attempted by 1992, namely, the use of insulating buffer layer on Si by Sugibuchi et al.², the use of non-oxide ferroelectric compatible with Si by Sinharoy et al.³, and the direct deposition of ferroelectric on Si⁴. Despite all these efforts, the reported f-FETs have not exhibited an acceptable memory retention as well as a low switching voltage.

We took an entirely different approach to solve the above problems, namely, the use of perovskite semiconductors that are chemically and crystallographically compatible with ferroelectric and which allow epitaxial hetero-structures^{1,5-6}. Moreover, it allows a simplest structure and a loose control of impurity and defects in conventional Si based technology. Therefore, it can be appropriate to a high density non-volatile memory that must compete partly with the disk memories. Additionally, an all-perovskite f-FET is one of vast possibilities which the perovskite semiconductors exhibiting the metal-insulator transition open. In this paper, we report performance of prototype all-perovskite f-FETs and discuss its advantages in the high density IC memory application.

2. BASIC STRUCTURES

There are an immense number of ferroelectric and semiconductive perovskites, and a suitable combination allows their lattice mismatch below 1%. The examples of semiconductive perovskites are (L,S)TO₃ system (L:rare earth element, S:alkaline earth element, T: 3d metal element) and HTSC's. The ferroelectricity was clearly observed in multilayers of (Pb,La)(Ti,Zr)O₃(PLZT)/ perovskites, where the perovskite were La_{2-x}Sr_xCuO₄ (x≤0.01) (LSCO), La_{1.75-x}Nd_{0.25}Sr_xCuO₄ (x ≤ 0.01), LaNiO₃, and La_{1-x}Sr_xCoO₃ (x≤0.01)⁷. Furthermore, in the LSCO films, a good control of conductivity and a good process stability were achieved.

Not only the prototype structure but also the practical device structures are markedly simple as shown in Figs.1.



FIG. 1 Device structures of a prototype (a), another prototype (b), and a practical (c). Ferro and semi denote the ferroelectric and the semiconducting channel.



FIG. 2 X-ray $2\theta-\theta$ scan (a) and pole figure plots (b) of $Bi_4Ti_3O_{12}/LSCO$ multilayers, which show the 3-dimensional alignment of each layers.

The result on the prototype f-FET that used a 20nm LSCO as a channel and a PLZT as a gate insulator was partly reported⁶. The gate area of the devices was approximately $50\mu m$ by $200\mu m$. It is worthwhile to mention that an even better crystallographic compatibility was obtained in $Bi_4Ti_3O_{12}/LSCO$ multilayers (Fig.2).

3. PROTOTYPE DEVICE PROPERTY

Figure 3 shows the short time memory retention and the write/erase repetition characteristics of a representative device, which is the first demonstration of the all-perovskite f-FET at room temperature (R.T.). Marked improvements in device performances were obtained as compared with the previous f-FETs: write/erase at \pm 7V with a pulse width < 0.1msec and a resistance modulation up to about 10%. The switching speed was estimated to be limited by a delay constant and can be improved to 1µs. What is more important, some devices retained a memory in an ordinary environment for an



FIG.3 Write/erase repeatability and short period memory retention of FET No.1 at R.T.. The spikes on the straight line near the abscissa show the timing and the polarity of write/erase pulses, where the upward and the downward spikes show the positive and the negative polarities, respectively. Ion/Ioff is the ratio of the measured current to the initial off-state current.



FIG. 4 Retention of an off-state of FET No.2 (a) and an on-state of FET No.3 (b), where the FETs No. 2,3 were on the same substrate and were fabricated in the same batch. The meanings of the spikes on the straight line and Ion/Ioff are same as in Fig.2.

exceptionally long time as compared with the previous reports. The off-state (low conductivity) was found to be stable (Fig.4(a)), and the on-state was less stable (Fig.4(b)). Then, the net resistance modulation decayed to approximately 50% of the initial value after 10 months.

4. HIGH DENSITY INTEGRATION

The obtained modulation is very low as a FET but can be comparable to the on/off ratio of the dynamic random access memory (DRAM) cell. The modulation can be improved by a few orders of magnitude by reducing the doping and the defects. However, this will be still by a few orders of magnitude lower than the modulation of typical MOSFETs. Moreover, we expect reduced switching speed for a low doping channel in the same feature size⁷. Therefore, the present f-FET had better use a switching transistor (ST) (Fig.1(c)), i.e., two-transistors/cell in integrated memory array. Nonetheless, it would not increase the number of ST in the memory cell more than in conventional f-FET. This is because the reported f-FETs need at least one ST anyway to circumvent the "half-select disturb pulse threshold" problem⁸.

The use of a ST increases the cell size. However, this cell should yield higher integration density than the capacitor type memory cells such as DRAM and FRAM. Moreover, the



FIG. 5 Schematic illustration of the structural change of typical memory devices by miniaturization. Water, the bucket, and the faucet corresponds to the electron gas, the capacitor, and the FET. The f-FET allows water leakage through the faucet and the capacitor.

on/off ratio of the ST in the present cell can be much lower than MOSFET in the DRAM, since ferroelectic itself can sustain the remnant polarization, and, therefore, the ST does not need to stop the constant current leakage. This favors reduction of the ST size, and facilitate the reduction of a total cell area furthermore. Additionally, unlike the f-FET that uses an insulating buffer layer, the memory retention of the present f-FET, which uses a ferroelectric directly formed on a semiconductor without an intermediate layer, is insensitive to the leakage current through the ferroelectric. Therefore, the present f-FET requires only a loose control of defects and impurities, contrarily to DRAM and E²PROM. It can also employ simple structures as shown in Figs.1 even in the 100nm-scale device due to the intrinsic incorporation of the SOI structure. This can be another advantage in fabrication processes over conventional Si-memories. These two features are the merits of the present f-FET to contribute significant reduction of the fabrication cost. The above discussion can be intuitively understood, if we regard the electron gas as water, a FET as a faucet, and a capacitor as a bucket as illustrated in Fig.5.

Our theoretical calculations suggest another problem of f-FETs that use an insulating buffer layer, additionally to the well-known high switching voltage problem and the above mentioned leakage-current problem. Namely, only a multi-domain polarization can be thermodynamically stable in ferroelectric/insulator/semiconductor structure (or ferroelectric/insulator/metal/ semiconductor structure). Contrarily, a mono-domain polarization can be stable in the present f-FET, which supports the high density integration.

We have discussed an integration scheme based on the performances of a preliminary prototype device. Our fabrication technology is not refined, and the optimization of material combination is on the way. Therefore, the all-perovskite f-FET can be much improved by further efforts. Though, the device characteristics will be still very different from the present Si memories. However, it is necessary for solid state devices to drastically simplify the memory cell structure, fabrication processes, and impurity control to enter a new field where disk memories dominate. Indeed, the present disk memories strive to identify weak fuzzy signals using the Partial Response Maximum Likelihood⁹ and the error correction.

5. CONCLUSION

We have reported the performances of prototype allperovskite f-FETs. Some devices retained memory over 10 months. The simple structure, which is unchanged even in 100nm size device, can reduce the number of process steps and simplify the processes. The defect- and impurityinsensitivity of the device does not require ultraclean facilities for the fabrication processes. These features can be advantageous in the high density IC memory application.

We have not yet explored the merits of epitaxial structure of the all perovskite f-FET. Although the polycrystal ferroelectrics do not exhibit hysteresis having a good squareness, single-crystal ferroelectrics are reported to do. Therefore, it may be possible to obtain a ferroelectric exhibiting a square hysteresis in the epitaxial all-perovskite f-FET. This would eventually solve the "half- select disturb pulse threshold" problem mentioned above.

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