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Optimization of Contact Process with Monte-Carlo Study for Advanced CMOS Devices

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1. Abstract

Inductive Coupled Plasma (ICP) soft etch instead of a conventional HF pretreatment, which is anisotropic etching with high density plasma and low incident energy, can uniformly removes native oxide at the bottom of a fine contact hole. Mechanism to form stable ohmic contact was theoretically analyzed by Monte-Carlo topological simulation. Using the ICP soft etch with low sputtering yield, it is possible to prevent from the resputtered deposition on the bottom of the hole. As a result, it is clarified that excellent ohmic characteristics, low Junction leakage current level and superior reliability of thin gate oxide can be achieved by using the ICP soft etch with optimized low bias voltage.

2. Introduction

As the packing density of CMOS circuit is greatly enhanced by using a interconnect scheme, a contact hole size must be scaled to smaller dimension. It becomes more difficult to form the stable ohmic contact with low resistance due to presence of nonuniform native oxide at the bottom of the contact holes[1]. Hydrofluoric acid (HF) treatment is a typical method to remove native oxide on a silicon substrate[2]. However, HF treatment gives rise to enlargement of the hole diameter and to formation of a visor structure of the contact hole by its isotropic nature. In a recent paper[3], it is reported that Si rich native oxide is formed at the surface of the silicon where damage is introduced by dry etching at the bottom of the contact hole. The paper reported further that, even by the HF treatment, it is difficult to remove completely the native oxide from the silicon surface. Requirements in pretreatment for CMOS application are uniformity in removal of native oxide by anisotropic etching, being low in ion energy and uniformity of the plasma distribution not to degrade the gate oxide reliability. One of the technologies which fulfills the requirements for CMOS application process is ICP soft etch (Fig. 1)[4]. In this study, the mechanism which brings the stable ohmic contact, was analyzed by Monte-Carlo topological simulation. It is clarified that resputtered deposition can be avoided by the optimization of sputtering yield in the ICP soft etch.

3. Monte-Carlo Study of Contact Process

Monte-Carlo simulation was useful in understanding the mechanisms removal of the native oxide in anisotropic etching. Sputtering yield Y depends on the energy E of incident ion which is determined by bias voltage.

$$Y(\text{atoms/ions}) = \frac{3\alpha}{4\pi^2} \times \frac{4m_i m_t}{(m_i+m_t)^2} \times \frac{E}{U_0} \qquad (1)$$

Here, mi and mt are masses of particles, α is a constant depending on the ratio mt / mi, and U_0 is surface binding energy of the material being sputtered. This expression of Y predicts that the yield will increase linearly with E. From this relation, the sputtering yield at an acceleration energy of 100eV in the ICP soft etch is 1 order of magnitude lower than that of the diode etching with 1000eV. Etching rate R is exposed as follows:

$$R \sim Y \times \Delta \qquad (2)$$

where Δ is density of plasma. The etching rate is affected by the density of plasma as well as by the bias voltage. The sputtered etching model used in the simulation is based on the concept described as follows. Ar ion erodes the substrate effectively in proportion to the cosine of incident angle of the ion. The sputtering yield is defined as the ratio of released atoms to total incident Ar ions. When Ar ion flux (Γ) which is proportional to Δ collides with substrate, a part of the flux

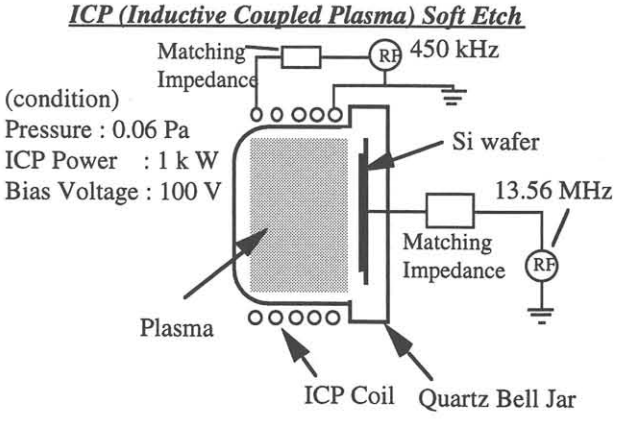

Fig. 1 ICP soft etch technology combines high density plasma with low incident energies[5].

generates sputtered species with a certain probability (Ps), an another part of the flux is reflected with a certain probability (Pr) and remaining part is stuck on the surface (Fig. 2). Here, flux (Is) of the sputtered species is given by

$$Is = Y\Gamma \qquad (3)$$

Further reflected Ar ion flux (Ir) on the surface, which is a part of the projected Ar ion flux, is described as follows:

$$Ir = Pr\Gamma \qquad (4)$$

and stuck Ar ion flux (In) on the surface, which is a part of the Ar ion flux, is given by

$$In = [1-(Ps+Pr)]\Gamma \qquad (5)$$

here,

$$Ps = \frac{Y}{K} \qquad (6)$$

where, K is a ratio of the number of sputtered species to the number of incident Ar ion relating to sputter.

Furthermore, a part of the sputtered species flux is going to stick on the substrate, and the others reflect with a certain probability.

Next, considering the sputtered species, the stuck species flux (Ss) and the reflected species (Sr) are expressed as a function of sputtered angle θ :

$$Ss = \Lambda Is(\theta) \qquad (7)$$

$$Sr = (1-\Lambda)Is(\theta) \qquad (8)$$

where, Λ is sticking coefficient. The parameters for this simulation are fitted using observed results by cross sectional TEM - EDX (Transmission Electron Microscopy - Energy Dispersive X-ray spectroscopy) analysis at the bottom of the contact hole. In the sample treated by low bias voltage, reacted Ti silicide was observed at the bottom of the contact hole (Photo 1-a). On the other hand, in the diode etching with the high bias voltage, an amorphous layer of 4 nm thickness, which includes silicon and oxygen was formed at the Ti/Si interface (photo. 1-b). A redeposited layer of 4 nm thickness is formed at the Ti/Si interface by the diode etching with the high bias voltage (1000eV) (Photo 1-b). This simulation model was applied to the contact holes having aspect ratio of 1.2, 3.0 and 6.0 with the native oxide of 10nm thickness. Using the ICP soft etch with low bias voltage (100eV), the native oxide at the bottom of the holes can be removed effectively even for the hole of high aspect ratio (Fig. 3a). In the high bias voltage (1000eV), the etching generates a significant amount of re-sputtered SiO_2 deposition on the bottom of the fine contact holes (Fig. 3b). This resputtered deposition from the sidewall strongly depends on the aspect ratio of holes. Using the ICP soft etch with low sputtering yield, it is possible to prevent from the resputtered deposition on the bottom of the hole with 0.1 μm diameter (Fig. 4a, 5a). On the other hand, high energy sputter etching with relatively high sputtering yields generates significant resputtered SiO_2 deposition (Fig. 4b, 5b). Namely, it is found that removed characteristics of the native oxide layer at the bottom of the hole depends on the sputtering yield. From these simulation results, It is clarified that low contact resistance can be achieved even for an advanced devices with the contact hole of 0.1 μm diameter by using the ICP soft etch with optimized low sputtering yield as a pretreatment step.

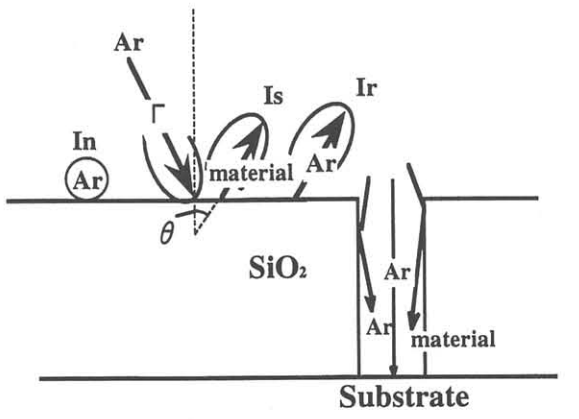

Fig. 2 Simplified schematic diagram of a sputter etching used in Monte-Carlo simulation.

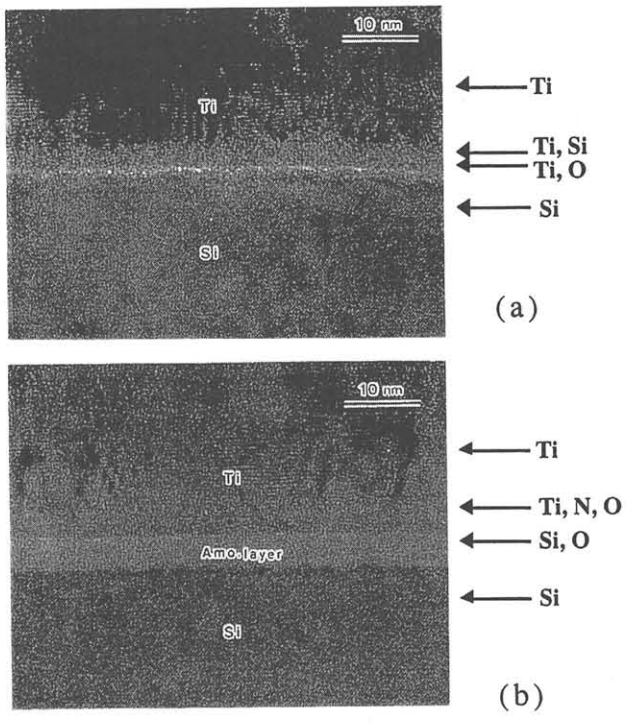

Photo. 1 Bright field cross sectional TEM micrograph and corresponding EDX and EELS (Electron Energy Loss Spectroscopy) analysis of a Ti/P^+ Si interface at the bottom of the contact hole.
(a) In the sample by the ICP soft etch, titanium reacts with Si.
(b) In the standard RF diode etch, an amorphous layer is formed at the Ti/Si interface.

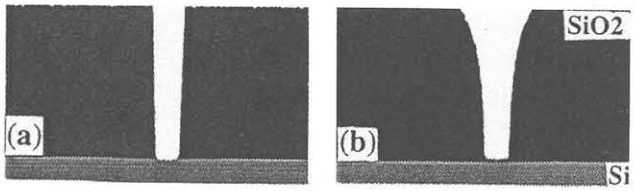

Fig. 3 Simulation results of sputter etching as a function of sputtering yield (aspect ratio:6.0).

(a) ICP soft etch avoids resputtered deposition.

(b) The RF diode etching with high sputtering yield generates a significant deposition of resputtered SiO_2.

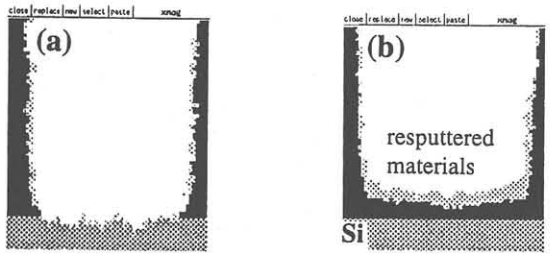

Fig. 4 Magnification of the bottom of the contact holes with 6.0 aspect ratio. (Simulation results)

(a) Using the ICP soft etch with low bias voltage, native oxide is removed.

(b) In the RF diode etching with high bias voltage, covered material is generated at the bottom of the hole.

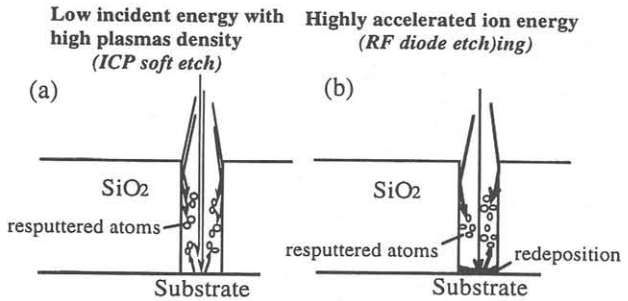

Fig. 5 High energy sputter etching generates a significant amount of resputtered SiO_2 deposition from side walls on the bottom of the contact hole.

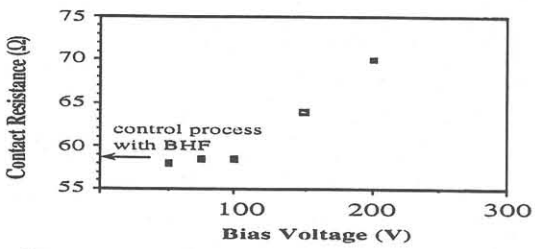

Fig. 6 P^+ contact resistance of 0.4 μm diameter as a function of bias voltage using ICP soft etch.

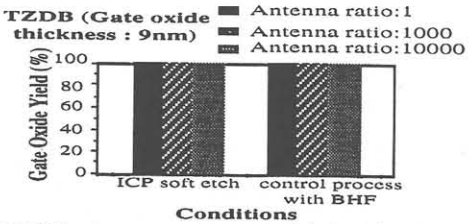

Fig. 7 MOS antenna structure were fabricated with various times the gate area ratio. The ICP soft etch yielded good results for the oxide film structure of 9nm thick.

4. Electrical Characteristics for CMOS Devices

A number of electrical evaluations on device characteristics were performed. A buffered HF (BHF) dip was used as control process. It is shown that the contact resistance depends on the bias voltage (Fig.6). Stable ohmic characteristics could be achieved by using the ICP soft etch with low bias voltage. The diode etching with high bias voltage results in the non-ohmicity of the contact due to SiO_2 deposition from sidewall on the bottom of the contact hole. The redeposited layer obstructs the current pass at the Ti/Si interface. Junction leakage currents of contacts by the ICP soft etch were suppressed to the leak level as that by the BHF treatment. In order to apply this to CMOS process, breakdown voltage of thin gate oxide was measured on 9nm gate oxide capacitor that was treated by each type of etch process. In a gate oxide breakdown test, the ICP soft etch process yielded significantly good results for 9nm gate oxide films (Fig.7). Therefore, the ICP soft etch with optimized conditions is an effective pretreatment method before metallization for advanced CMOS devices.

5. Conclusions

In summary, the ICP soft etch is an effective in-site pre-metallization process at the contact hole. It is clarified from the result of Monte-Carlo simulation that the ICP soft etch can suppress resputtered deposition from intermetal dielectric even for the hole of 0.1 μm diameter. Utilizing the ICP soft etch for a CMOS device, electric characteristics such that excellent ohmic characteristics, superior reliability of thin gate oxide is obtained.

Acknowledgments

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