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New Characterization of $TiSi_2$ Local Wiring Technology and Its Impact on Low Power / High Speed Quarter Micron CMOS

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A $TiSi_2$ local wiring technology is newly characterized. It is revealed abrupt increase in sheet resistance at submicron narrow line of $TiSi_2$ film occurs in a-Si/Ti system. It is suggested, As-atom easily diffuses from Si to $TiSi_2$ and $TiSi_2$ to Si, on the other hand, B atom easily diffuses from Si to $TiSi_2$ but hardly diffuses from $TiSi_2$ to Si. The $TiSi_2$ local wiring technology is applied to quarter micron CMOS. More than 20% of reduction in power dissipation and 32ps propagation delay time are obtained.

1. INTRODUCTION

A $TiSi_2$ local wiring technology is effective to reduce parasitic junction capacitance and resistance simultaneously[1], which is one of the key technologies for quarter micron device and beyond. In Fig. 1, junction capacitance per inverter is calculated as a function of power supply voltage. It indicates that in a conventional structure, junction capacitance markedly increases by reducing power supply voltage, and in a local wiring structure, such a increase in junction capacitance can be suppressed.

However, for application of this technology, careful attentions are required on silicidation reaction or dopant behavior. Previous reports of the SALICIDE scheme revealed increase in sheet resistance of a narrow line[2], or shifts of the threshold voltage due to lateral dopant diffusion in the dual gate CMOS[3].

We report for the first time the abrupt increase in sheet resistance at submicron narrow line of $TiSi_2$ film occurs also in the a-Si/Ti system, as well as in the Ti/Si-substrate or Ti/poly-Si system. We characterize the $TiSi_2$ local wiring technology with new test patterns. The interdiffusion of As-atom from n^+ layer to p^+ layer via $TiSi_2$ local wiring layer increases the leakage current of p^+/n junction. It is revealed marked increase in leakage current of both n^+/p and p^+/n junction occurs with test pattern of huge ratio of local wiring area and active area. We propose a new interdiffusion model that As-atom easily diffuses from n^+ layer to $TiSi_2$ and $TiSi_2$ to p^+ layer, on the other hand, B atom easily diffuses from p^+ layer to $TiSi_2$ but hardly diffuses from $TiSi_2$ to n^+ layer. We apply the $TiSi_2$ local wiring technology in quarter micron CMOS, and results in a successful reduction of power dissipation and propagation delay time due to the reducion of parasitic junction capacitance.

2. EXPERIMENTAL

$TiSi_2$ local wiring layer is fabricated as follows. Firstly, 90nm a-Si film and 40nm Ti film are *in-situ* deposited by DC magnetron sputtering. Secondly, the a-Si film of local wiring region is patterned by photolithography and etching. Finally, it is converted to the 100nm $TiSi_2$ film with the 10nm residual a-Si film at the top by 2step RTA in N_2 ambient. The residual a-Si film on the top of $TiSi_2$ is successfully removed during opening contact windows.

Junctions of the n^+/p and p^+/n types are fabricated before local wiring layer formation. In the n^+ and p^+ layer, $5x10^{15}cm^{-2}$ of As^+ and BF_2^+ ions are implanted and diffused by RTA at 1050°C, 10s, in N_2 ambient. After $TiSi_2$ local wiring layer is fabricated, dielectric layer is deposited and post silicidation annealing is employed with 800°C, 20min, in N_2 ambient.

Sheet resistance of $TiSi_2$ local wiring layer is evaluated with test patterns fabricated on thermal oxide. Dopant-interdiffusion between n^+ and p^+ layer is evaluated with test patterns of n^+/p and p^+/n junctions, which is connected each other via $TiSi_2$ local wiring layer. Dopant-redistribution from Si to $TiSi_2$ is evaluated with test patterns of n^+/p and p^+/n junctions with various ratio of local wiring area and active area.

3. RESULTS AND DISCUSSION

Firstly, the narrow line effect of a-Si/Ti system is examined. Fig. 2 shows the sheet resistance of $TiSi_2$ film as a function of line width. Abrupt increase in sheet resistance accompanied with narrowing line width is revealed. This result is similar to that reported in the Ti/Si-substrate or Ti/poly-Si system [2].

In comparison between a-Si/Ti and Ti/Si-substrate or Ti/poly-Si system from silicidation reaction, two common characteristics are extracted. One is that Si region is restricted by photolithography and etching, on the other hand, Ti region is extended to whole wafer area before silicidation. Another is that dominant diffusion species in silicidaton reaction is Si atom[4]. Hence, it is deduced the narrow line effect on Ti/Si system is due to limited diffusion species.

Secondly, effects of dopant-interdiffusion is vertified. Fig. 3 shows the leakage current of junction with interconnecting n^+ and p^+ layer by $TiSi_2$ local wiring. In n^+/p junction, leakage current doesn't increase with interconnecting n^+ and p^+ layer by $TiSi_2$ local wiring. On the other hand, in p^+/n junction, leakage current increases with interconnecting, and further increases by closing the distance between n^+ and p^+ layer. This result suggests p^+/n junction is degraded due to interdiffusion of As-atom from n^+ layer to p^+ layer via $TiSi_2$ local wiring layer. However, it is necessary to check the pitting[5] of Si-substrate, which may also induce junction leakage current. The $TiSi_2$/Si interface is observed by SEM after removal of $TiSi_2$ film by HF solution. No local consumption of the substrate or pitting of Si-substrate is observed for both n^+ and p^+ layer covered with local wiring. Moreover, the $TiSi_2$/Si interface covered with local wiring is more flat compared with that not covered. This result indicates that in a-Si/Ti/Si-substrate system, Ti atom reacts dominantly with a-Si. Therefore, increase in leakage current at p^+/n junction with interconnection in Fig. 3 is due to interdiffusion of As-atom rather than pitting of Si substrate.

We also investigated the dopant behavior with new patterns, these are varied the ratio of local wiring area and active area. Fig. 4 shows the junction leakage current as a function of ratio of local wiring area and active area. In both n^+/p and p^+/n junction, with increasing the ratio to more than 1000, leakage current markedly increases. With a junction of the ratio one or two doesn't show such a leakage current. Marked increase in leakage current of ratio more than 1000 suggests that the depletion layer extends to the $TiSi_2$/Si interface due to dopant concentration lowering to one thousandth, where silicidation induced defects generating leakage current. We verified the $TiSi_2$/Si interface by SEM as same as the test patterns of interdiffusion. Althougt the $TiSi_2$/Si interface covered with local wiring is as rough as not covered one, no pitting of Si-substrare is observed. This result suggests lowering of dopant concentration with pattern of ratio more than 1000 is due to dopant-redistribution from Si to $TiSi_2$[6], rather than consumption of highly doped active area.

In Fig. 5, we propose a new model of dopant-interdiffusion, from the results of Fig. 3 and 4. The dopant-interdiffusion is divided into two stages, 1st stage is diffusion from Si to $TiSi_2$, 2nd is from $TiSi_2$ to Si. As-atom easily diffuses from Si to $TiSi_2$ and $TiSi_2$ to Si, on the other hand, B atom easily diffuses from Si to $TiSi_2$ but hardly from $TiSi_2$ to Si. It is a common characteristics to As and B atom that diffusion from Si to $TiSi_2$ occurs. The difference is that As can diffuse from $TiSi_2$ to Si, on the other hand, B is fixed in $TiSi_2$ due to stable compound TiB formation[7] and cannnot diffuse to Si.

Finally, we demonstrate the impacts of the $TiSi_2$ local wiring technology for device performance. Power dissipation and propagation delay time is evaluated by 101 stages ring oscillator. In MOSFETs with local wiring, contact windows are opened on the field oxide, which enables the reduction of source/drain width from 1.8 to 0.4μm. Fig. 6 shows the propagation delay time as a function of power supply voltage. As a result of source/drain-width reduction by local wiring, 15% of speed improvement at 0.35μm CMOS, 3.3V is obtained and propagation delay of 32ps at 0.25μm CMOS, 3.3V is obtained. Fig.7 shows the ratio of decrease in power dissipation as a function of power supply voltage. Noticiable point is that the reduction of power dissipation by local wiring is more effective at low voltage, and more than 20 % of reduction is obtained at 1V.

4. CONCLUSION

It is revealed for the first time the abrupt increase in sheet resistance at submicron narrow line of $TiSi_2$ film also occurs in a-Si/Ti system. We propose a new interdiffusion model. As-atom easily diffuses both from Si to $TiSi_2$ and $TiSi_2$ to Si, on the other hand, B atom easily diffuses from Si to $TiSi_2$, but hardly diffuses from $TiSi_2$ to Si. It is also demonstrated the $TiSi_2$ local wiring technology actually reduces the parasitic junction capacitance, results in a successful reduction of power dissipation and propagation delay time in quarter micron CMOS.

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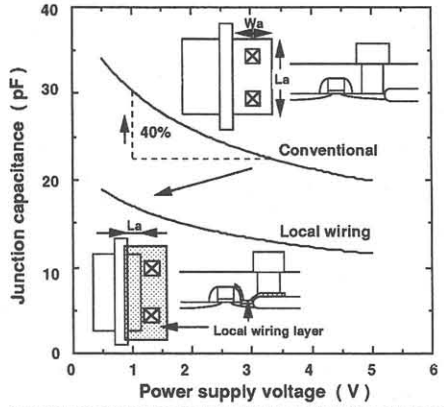

Fig. 1 Junction capacitance per inverter as a function of power supply voltage. Wa=1.5μm, La=6μm for conventional structure, Wa=0.5μm, La=6μm for local wiring structure.

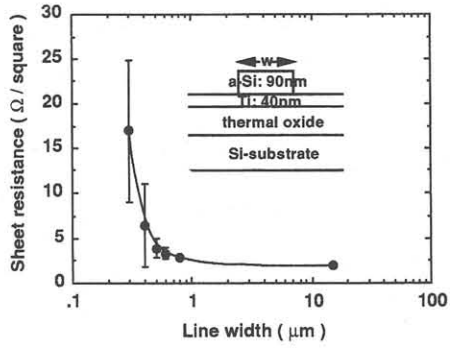

Fig. 2 Sheet resistance of $TiSi_2$ film as a function of line width

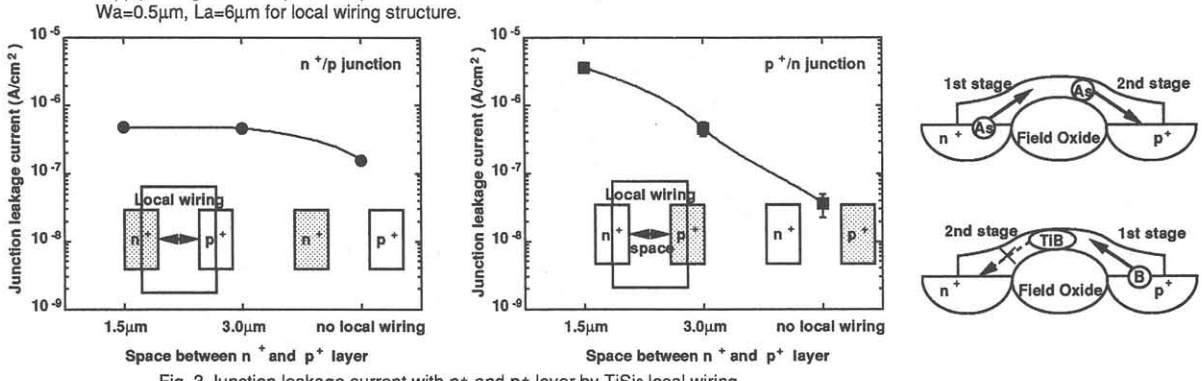

Fig. 3 Junction leakage current with n+ and p+ layer by $TiSi_2$ local wiring. Leakage current is measured at reverse bias of 3.3V

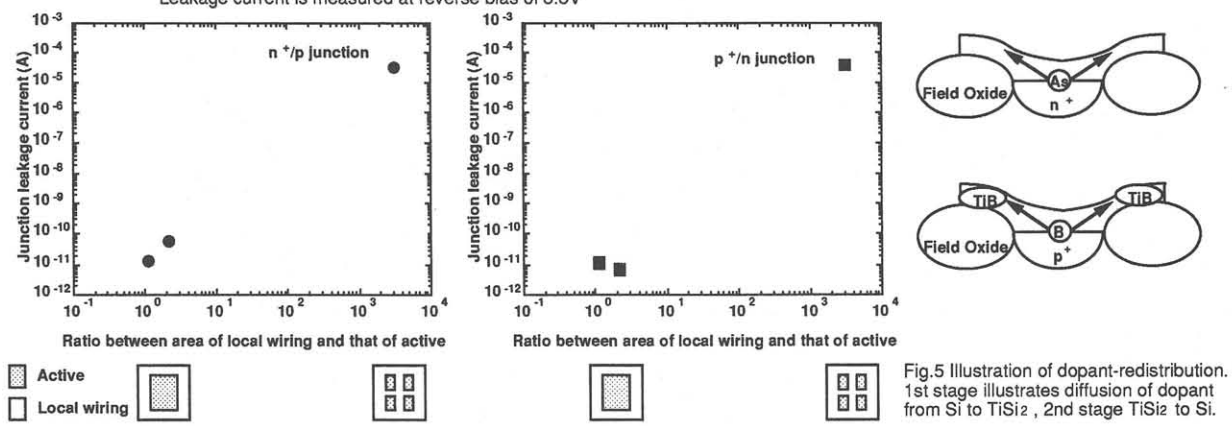

Fig.5 Illustration of dopant-redistribution. 1st stage illustrates diffusion of dopant from Si to $TiSi_2$, 2nd stage $TiSi_2$ to Si.

Fig. 4 Junction leakage current as a function of ratio between area of local wiring and that of active. Leakage current is measured at reverse bias of 3.3V

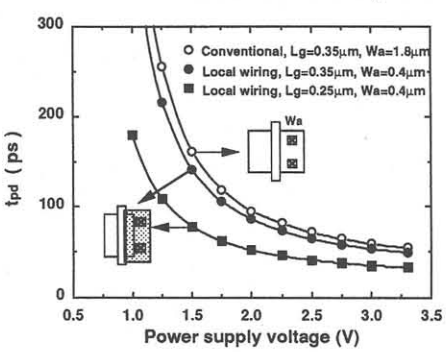

Fig. 6 Propagation delay time as a function of power supply voltage measured by 101stages ring oscillator.

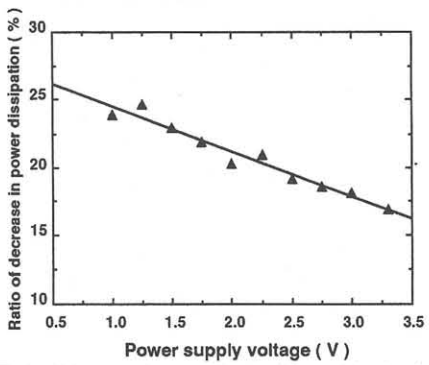

Fig. 7 Ratio of decrease in power dissipation applying local wiring as a function of power supply voltage. Power dissipation is measured by 101 stages ring oscillator. Gate length is 0.35μm, active width is 1.8μm for conventional, 0.4μm for local wiring structure.