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High-Speed and Low-Power Interconnect Technology for Sub-Quarter-Micron ASICs

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The optimum interconnect structure for high-speed and low-power sub-quarter-micron ASICs is investigated. High-speed and low-power scaling rules for the interconnect structure are extracted statistically from wiring data in ASICs. A 0.25-μm interconnect structure is fabricated based on the scaling rules and using organic SOG (Spin-On-Glass) as a low-dielectric-constant interlayer insulator. This structure reduced the gate delay by 39% and the gate power by 47% compared to a conventional structure.

1. Introduction

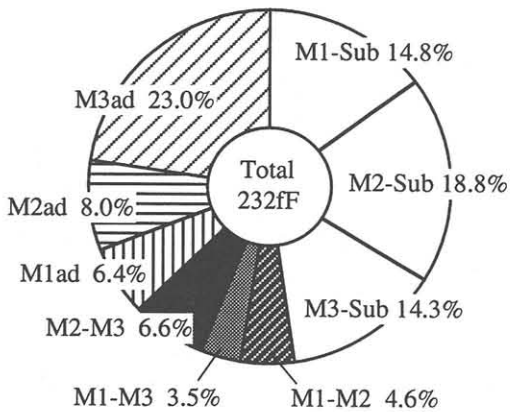
In modern CMOS ASICs scaled down to a half-μm or finer technology, interconnect delay is an important factor in determining the total gate delay. The interconnect delay caused by wiring capacitance and wiring resistance increases as the technology is scaled down, and will soon become larger than the transistor delay. In terms of gate power, reducing the wiring capacitance is also important, because gate power is proportional to the total capacitance in a circuit, and the wiring capacitance accounts for more than half of the total capacitance.

In this paper, the optimum interconnect structure for high-speed and low-power ASICs is discussed. At first, changes in the capacitance components of an ASIC that accompany a conventional scaling are analyzed based on a statistical wiring data. Next, high-speed and low-power scaling rules for the interconnect structure are extracted. Finally, a interconnect structure for 0.25-μm ASIC is fabricated according to the scaling rules and using organic SOG as a low-dielectric constant interlayer insulator.

2. Scaling of Interconnect Structure

Wiring capacitance components extracted from wiring data of 3 examples of actual 0.5-μm ASIC gate arrays are shown in Fig. 1. Adjacent capacitance of the third metal layer has the largest contribution to the total wiring capacitance even at 0.5-μm technology. The sum of the adjacent capacitance of each metal layer is 37.4%, which is over one-third of the total wiring capacitance.

Wiring capacitance is determined mostly by the adjacent capacitance below 0.3-μm technology, which is affected little by the interlayer insulator thickness. Changes in the capacitance components of an ASIC logic gate caused by conventional scaling are analyzed from 1-μm to 0.1-μm technology (Fig. 2). Wiring capacitance is calculated using Chern's formula [1]. The wiring length and gate width are proportional to the scaling factor (Optical shrink) in this analysis. Line-to-substrate capacitance (Cs) and cross over capacitance (Cc) are reduced with scaling down, because all of the horizontal sizes are



Average-length wiring = 1.4 mm
M*n*ad: Adjacent capacitance in *n*th metal layer

Fig. 1. Wiring capacitance components extracted from 0.5-μm ASIC gate arrays.

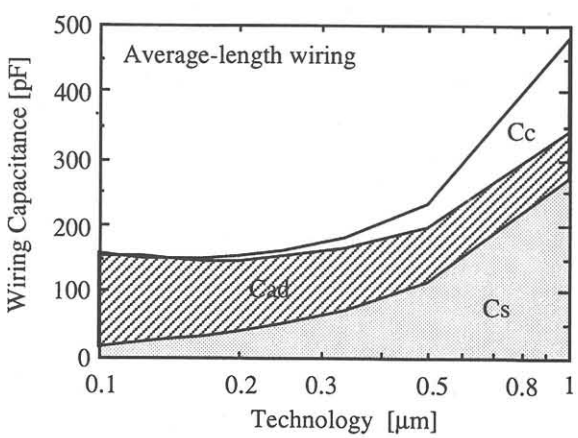


Fig. 2. Dependence of the wiring capacitance component on fabrication technology in average-length wiring.

scaled down. On the other hand, adjacent capacitance (Cad) becomes larger as a result of scaling down, because the space between adjacent wirings narrows while the vertical size remains constant.

3. High-speed and Low-power Scaling Rules for Interconnect Structures

According to the analysis above, conventional scaling will lead to an increase in adjacent capacitance because of the closely packed wiring. There must be a more suitable scaling rule for interconnect structures instead of conventional scaling. An ideal interconnect scaling rule for high-speed and low-power ASIC is considered independent of various fabrication issues.

The interconnect scaling rule assumes that the interlayer-insulator thickness is scaled with k^h, and the metal thickness is scaled with k^t, where k is a scaling factor. Figure 3 shows the dependence of gate delay on the scaling parameters h and t calculated using the wiring data after scaled down to 0.25-μm technology.

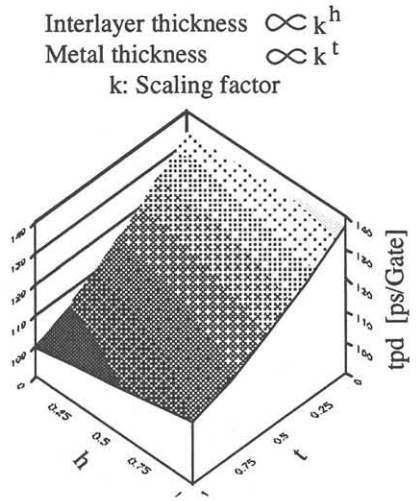


Fig. 3. Dependence of gate delay on scaling parameters h and t after scaling down to 0.25-μm.

The fastest scaling rule for average-length wiring is to keep the interlayer-insulator thickness constant and scale the metal thickness proportional to the scaling factor (h=0, t=1). The interlayer-insulator thickness has little effect on tpd but the metal thickness has a large effect on tpd. Wiring capacitance increases with metal thickness, and the wiring resistance decreases with metal thickness. Thus, the result means that wiring capacitance has a greater effect on gate delay than wiring resistance has. The gate power has a similar dependence on h and t and the lowest-power scaling rule is the same (h=0, t=1).

4. Experimental Results in a 0.25-μm Interconnect Structure

The optimum interconnect structure for a 0.25-μm ASIC was fabricated based on the proposed scaling rules and using organic SOG as a low-dielectric-constant interlayer insulator (Fig. 4). Tungsten plugs were used for contact between the metal layers so that the interlayer-insulator thicknesses were the same as in a 0.5-μm technology. The metal thicknesses were reduced to half those of a 0.5-μm technology. Organic SOG interlayers were used to reduce adjacent wiring capacitances [2, 3]. The thin 50-nm-thick P-TEOS layer under the organic-SOG layer provides adhesion between the metal and the organic SOG. The P-TEOS layer over the organic SOG protects the organic SOG from etching of the upper metal.

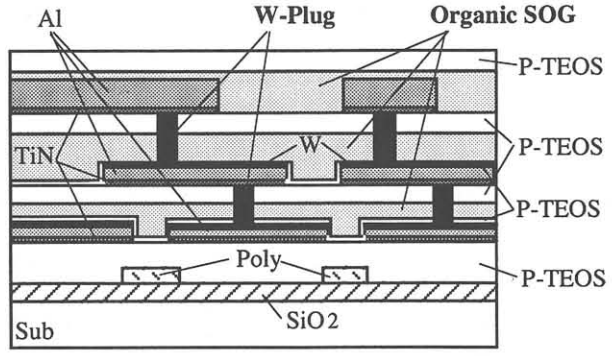


Fig. 4. Schematic cross section of a fabricated interconnect structure for a 0.25-μm ASIC.

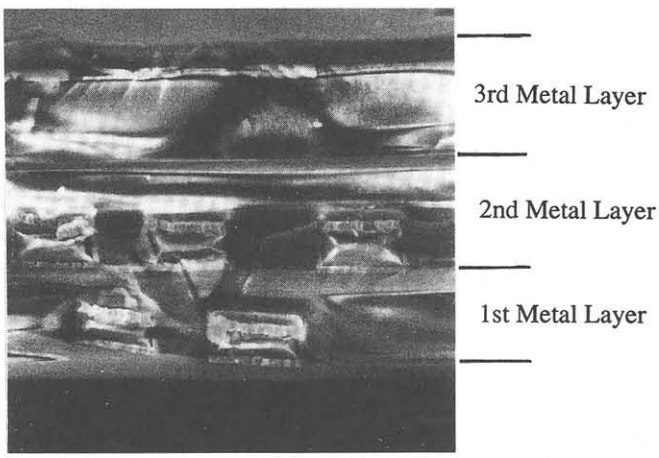


Fig. 5. SEM photograph of a cross section of the fabricated interconnect structure.

A cross-section SEM photograph of the fabricated interconnect structure is shown in Fig. 5. Because of the high fluidity of the organic SOG, adequate local-area planarization was achieved without planarization process steps. The adjacent capacitance was reduced by 35% from that of a conventional interconnect structure using P-TEOS interlayer insulators. Figure 6 shows the dependence of the adjacent capacitance on the metal-spacing. The measured capacitance agrees well with

Chern's model [1] assuming the equivalent dielectric constant of 3.0.

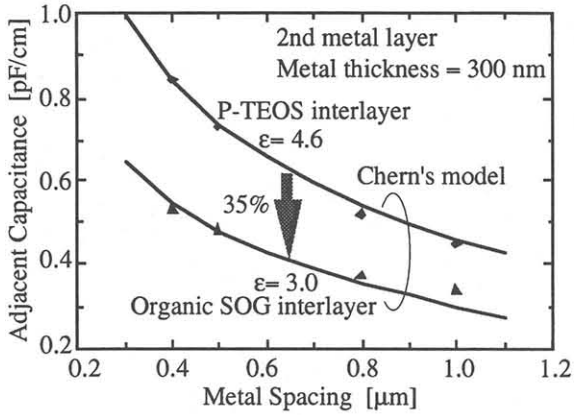


Fig. 6. Measured adjacent capacitance as a function of metal spacing.

Calculated gate delay from the measured wiring capacitance and resistance is shown in Fig. 7. In conventional scaling, the gate delay is almost constant below 0.3-μm technology due to the increase in wiring capacitance. On the contrary, adopting the high-speed and low-power scaling rule allows the gate delay to be reduced down to 0.15-μm technology; at this point the effect of wiring resistance appears. Gate delay at 0.25 μm technology was reduced by 23% by adopting the scaling rule, and reduced by 21% by using organic SOG, for a total, gate delay reduction was 39%.

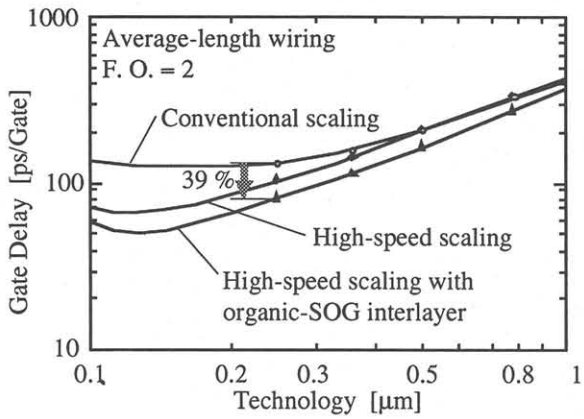


Fig. 7. Calculated gate delay from measured wiring capacitance and resistance.

The gate power calculated from the measured wiring capacitance and resistance is shown in Fig. 8. In conventional scaling, the reduction in gate power becomes slower below 0.3 μm. Adopting the high-speed and low-power scaling rule, the gate power is reduced in proportional to the square of the design rule down to 0.1-μm technology. The gate power is reduced by 31% by adopting the scaling rule with 0.25-μm technology, and reduced by another 25% by using organic SOG. Altogether, the gate power is reduced by 47% compared to a conventional structure.

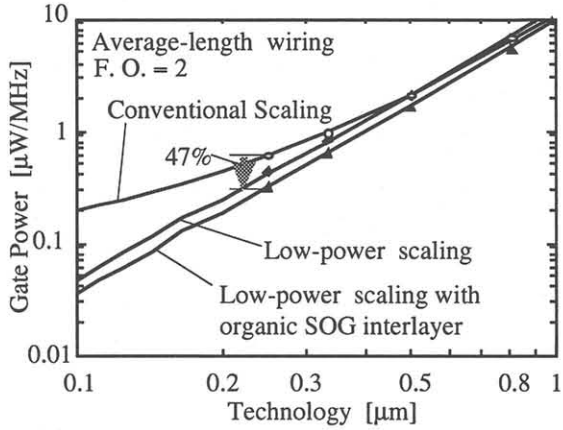


Fig. 8. Calculated gate power from measured wiring capacitance and resistance.

5. Conclusion

The optimum interconnect structure for a high-speed and low-power for sub-quarter-micron ASICs was investigated. The highest-speed and the lowest-power scaling rules for an average-wiring length interconnect are to keep the interlayer-insulator thickness constant while scaling the metal thickness proportional to the design rule. This result indicates that the adjacent wiring capacitance has a greater effect on gate delay than the wiring resistance has for average-length wiring.

A 0.25-μm interconnect structure was fabricated based on the interconnect scaling rule and using organic SOG as a low-dielectric-constant interlayer insulator. The new interlayer structure reduced the adjacent capacitance by 35% compared to a conventional interconnect structure. Adopting the scaling rule for a 0.25-μm ASIC enables to reduce the gate delay by 23% and the gate power by 31% compared to a conventional scaling. Totally, the gate delay was reduced by 39% and the gate power was reduced by 47% compared to a conventional interconnect structure.

Acknowledgments

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